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FET INPUT VOLTAGE AMPLIFIER FOR LOW FREQUENCY NOISE MEASUREMENTS

Krzysztof Achtenberg, Janusz Mikołajczyk, Zbigniew Bielecki

Military University of Technology, Institute of Optoelectronics, Gen. S. Kaliskiego 2, 00-908 Warsaw, Poland
(✉ *krzysztof.achtenberg@wat.edu.pl*, +48 261 839 523, *janusz.mikolajczyk@wat.edu.pl*, *zbigniew.bielecki@wat.edu.pl*)

Abstract

The paper presents a low noise voltage FET amplifier for low frequency noise measurements. It was built using two stages of an op amp transimpedance amplifier. To reduce voltage noise, eight-paralleled low noise discrete JFETs were used in the first stage. The designed amplifier was then compared to commercial ones. Its measured value of voltage noise spectral density is around 24 nV/$\sqrt{\text{Hz}}$, 3 nV/$\sqrt{\text{Hz}}$, 0.95 nV/$\sqrt{\text{Hz}}$ and 0.6 nV/$\sqrt{\text{Hz}}$ at the frequency of 0.1, 1, 10 and 100 Hz, respectively. A −3 dB frequency response is from ~ 20 mHz to ~ 600 kHz.

Keywords: low noise amplifier, low frequency noise measurements, field effect transistors, FET voltage noise, FET input amplifier.

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1. Introduction

Instrumentation for a *low frequency noise measurements* (LFNM) is a tool used to characterize a wide spectrum of devices [1]. It is applied in many technologies, *e.g.*, semiconductors [2, 3], microelectronic materials [4–10], electro-chemical devices [11], photodetectors [12–18], as well as other materials [19–21]. In this research, some special amplifiers (*ultra-low noise amplifier* – ULNA) are widely used. Their performances are also utilized in detection technology [22, 23] (as preamps in sensor signal conditioning) or in characterization of other low noise instruments [24–27].

However, the design of such amplifiers requires performing noise analyses of their components and selecting a configuration of both passive and active elements. At first, the choice between *bipolar junction transistor* (BJT) and *field effect transistor* (FET) technologies should made. BJTs are characterized by lower voltage noise and higher current noise caused by a high base current [26]. In this case BJT input current noise increases with the base current needed to set transistor's operating point in an active region and to obtain high gain (a current gain coefficient depends on the base current as well). Using this technology, lower impedance of the amplifiers' input can be obtained. However, these amplifiers require applying unstable electrolytic capacitors in AC

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coupling filters. Considering performances of BJT devices, FET technology is more effective in many low-noise signal applications. Nowadays, some novel low-noise FET transistors with a large area of the gate have voltage noise comparable with that of BJTs and the input bias current at the level of pA.

In order to perform noise estimation of a FET amplifier, there is a need to analyze its noise sources (Fig. 1).

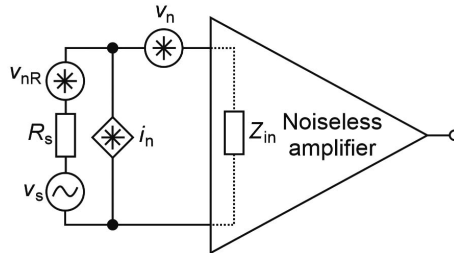

Fig. 1. Noise model of the amplifier.

In Fig. 1, v_n and i_n are equivalent input voltage and current noises of the analyzed amplifier and v_nR is the thermal noise of the source resistance R_s. For uncorrelated noise sources, the equivalent input voltage noise v_ni is described by:

$$v_\text{ni} = \sqrt{4kTR_\text{s} + v_\text{n}^2 + i_\text{n}^2 R_\text{s}^2}\,. \tag{1}$$

For a *junction field effect transistor* (JFET), voltage noise v_nJFET is represented mainly by its $1/f$-noise and channel thermal noise. It can be calculated from the equation:

$$v_\text{nJFET} = \sqrt{v_{1/f}^2 + 4kT\left(\frac{2}{3}\frac{1}{g_\text{m}}\right)}, \tag{2}$$

where k is the Boltzmann constant, T is absolute temperature, and $2/(3g_m)$ is approximated resistance of the JFET channel. Since g_m rises with the drain current I_D, therefore, v_nJFET is proportional to $1/I_D^{1/4}$ [29]. And for high current I_D, the influence of v_nJFET decreases. However, there are observed both degradation of JFET's parameters and generation of an additional noise caused by, $e.g.$ substantial instabilities at high heating and temperature dissipation. When a JFET works with a high drain-gate voltage V_{DG}, the gate current I_G can increase many times. The gate leakage current component is also noticed. This extra *ionization-collision* current is proportional to the current I_D. Its value increases exponentially with both temperature and voltage V_{DG}. As a result, the JFET total current noise increases mainly due to the shot noise of the gate current described by:

$$i_\text{nJFET} = \sqrt{2qI_\text{G}} = \left(3.2 \cdot 10^{-19} I_G\right)^{1/2}, \tag{3}$$

where q is the elementary charge.

In order to obtain a low noise level, a special construction of amplifier is needed. For example, some voltage ULNAs constructed using low noise JFETs can be found in the literature [30–32]. A special amplifier consisting of some discrete JFETs is described in paper [33]. Its noise is around 1.4 nV/$\sqrt{}$Hz and 0.6 nV/$\sqrt{}$Hz for the frequencies of 1 Hz and 10 Hz, respectively. Another interesting design implementing some additional amplifiers characterized by well-known gain and

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a specific calibration method is described in [34]. There was applied an amplifier input stage with some paralleled transistors. Its equivalent input voltage noise was reduced by factor $\sqrt{n}$ where n is the number of paralleled transistors [35]. Its noise level was similar to that of amplifiers in which some special and more expensive transistors were used.

2. JFET voltage noise measurements

During the selection of ULNA's components, some tests of JFET samples were performed. In the first research step, some inexpensive and popular JFETs such as BF862, 2SK3557-6, 2SK208-GR or 2SK209-GR were used. The measurement task was to define their total input voltage noise at the RT temperature determined for these tests. The testing setup consisted of a JFET amplifier (common source configuration) and a low-noise buffer (ADA4625). To set current I_D and voltage V_{DS} in the active region of transistor operation, a drain resistance R_D was selected. The total voltage gain A_V was determined using a HAMEG HM8150 signal generator (Fig. 2a). The gain values were comparable to theoretical ones resulting from the transconductance value g_m of the tested JFETs.

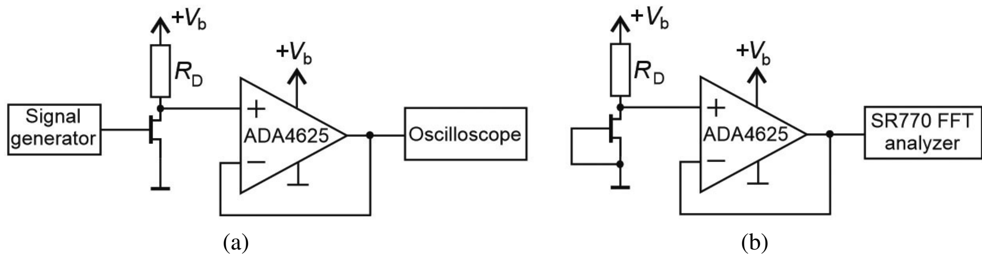

Fig. 2. Measurement setup for the total A_v gain (a) and the output noise (b).

The transistor gate was connected to the ground to determine the output *voltage spectrum density* (VSD) (Fig. 2b). It was measured using an SR770 FFT network analyzer (Stanford Research). The analyzer has the input reference voltage noise of 5 nV/$\sqrt{\text{Hz}}$ at 1 kHz. These tests were performed for the frequency range from 0.6 Hz to 10 kHz and for the supply voltage V_b of 12 V (lead–acid battery).

The noise measured spectra for these low noise JFETs are shown in Fig. 3. Parameters of the JFETs' operating points on the basis on which their input voltage noises were calculated are listed in Table 1.

Table 1. Parameters of the tested common source amplifier JFETs.

JFET	I_D [mA]	V_{DS} [V]	g_m [mS]	$A_V(g_m \cdot R_D)$	R_D [Ω]	Manufacturer
BF862	14	5.71	35.57	17.79	500	NXP
2SK3557-6	13.47	3.3	22.03	16.52	750	ON Semi.
2SK208-GR	4.33	4.09	3.10	6.19	2k	Toshiba
2SK209-GR	5.27	2.18	12.22	24.4	2k	Toshiba

The measured VSD level in the case of BF862 corresponds to the catalogue one. The frequency corner has the value of about 1 kHz. In the frequency range of a few kHz, the voltage noise is of

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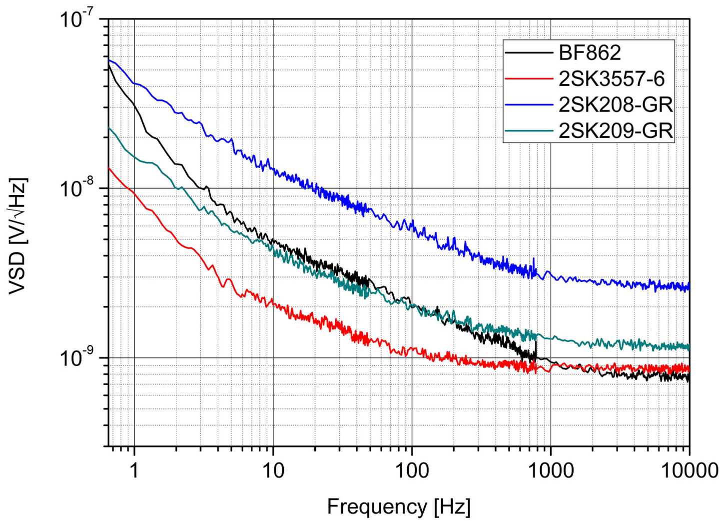

Fig. 3. Voltage spectral density of noise for BF862, 2SK208-GR, 2SK209-GR and 2SK3557-6.

0.8 nV/√Hz. Moreover, this transistor is characterized by high transconductance in the range of 35–45 mS. That is why, it is a popular active component used in low noise amplifiers. Despite the high frequency corner, this transistor makes it possible to obtain high voltage gain in a common source amplifier. For the tests of 2SK3557-6 JFETs, the results were similar to the old model 2SK170-BL. In comparison, these JFETs are cheap and have the lowest level of $1/f$ corner frequency (of about 300 Hz) with high transconductance up to 35 mS. Their measured VSD is of around 9 nV/√Hz at the frequency of 1 Hz and is lower in comparison with BF862. At higher frequencies, that noise relation is exchanged.

The noise spectra of 2SK3557-6 JFET for different operating points (bias voltages) were also measured (Fig. 4). During these tests, its gate was connected to the ground using a paralleled 10

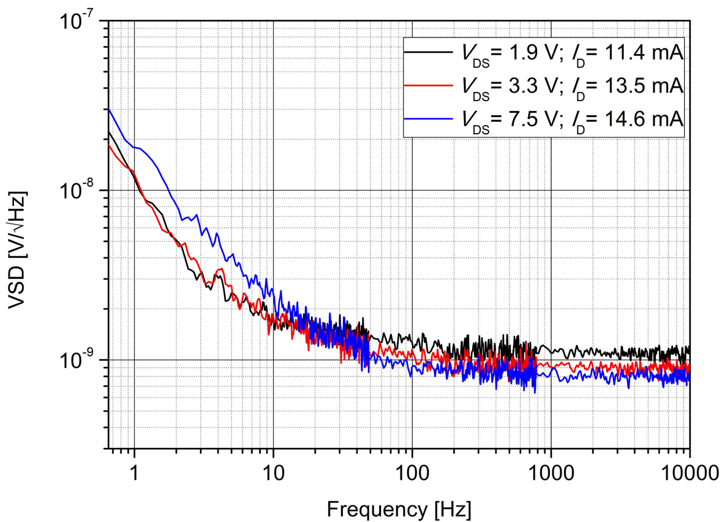

Fig. 4. VSD of 2SK3557-6 for different bias voltages.

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MΩ resistor and a 10 μF polyester capacitor (WIMA MKS2). In that case, there was not noticed any input current noise of the JFET. The output voltage noise was dominated by v_{nJFET} For the maximal drain current of 14.6 mA, both highest transconductance of about 28 mS and lowest thermal noise of its channel (according to Eq. (2)) above 100 Hz were obtained. However, at low frequencies, a higher $1/f$ noise component was observed through comparing spectra obtained for lower values of the drain current and the drain-source voltage. Low levels of I_D and V_{DS} voltage reduced g_m and the same time increased the channel thermal noise. The optimum results were received for the voltage V_{DS} of about 3 V.

Another amplifier configuration is based on some paralleled JFET transistors. Its disadvantage is increase in its input capacitance. Therefore, the total input capacitance should be considered during the selection of the number of paralleled transistors. While using cheap and more available JFETs, this design requires more work to build a low noise amplifier. There are also some transistors with much lower noise available on the market, but their price is also higher. The literature analysis shows that the best ones are IF9030 or IF3601 (InterFET technology). The noise level of the IF9030 type is from 1.5 nV/√Hz at 1 Hz to 0.5 nV/√Hz at 10 kHz [36]. The other one has lower noise at high frequencies but a higher input capacitance of 300 pF.

3. Low noise voltage amplifier

Basing on the performed analyses, a low noise voltage amplifier with the selected 2SK3557-6 JFETs was designed. Its input was modified using eight-paralleled transistors. It offered the noise level of 0.6 nV/√Hz at the frequencies above 100 Hz. The transistors' drains were supplied through R_2 and R_7 resistors using a 12 V/7 Ah lead–acid battery. To minimize voltage fluctuations that battery, there were used some 22 μF tantalum capacitors. The schematic diagram of this amplifier is shown in Fig. 5.

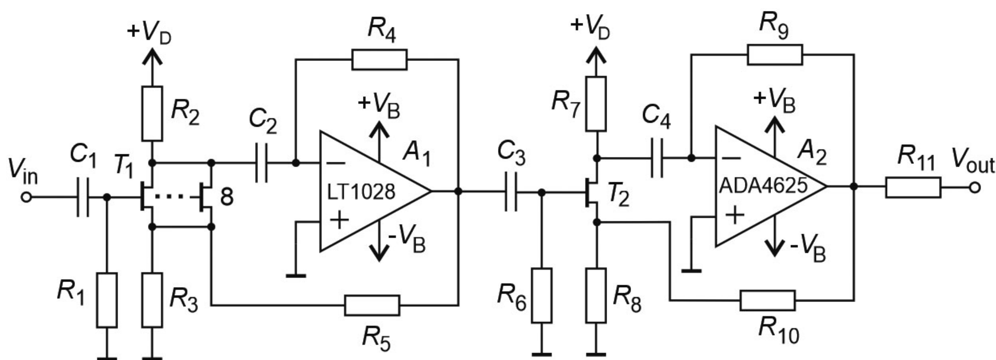

Fig. 5. Scheme of the ultra low noise amplifier with a JFET input stage.

The amplifier is composed of two AC-coupled stages. Each stage contains a discrete JFET amplifier at the input of transimpedance amplifier. The open loop gains are $g_{mT1}R_4/(1 + R_3 g_m)$ and $g_{mT2}R_9/(1 + R_8 g_m)$ for the first stage and the second stage, respectively. The values of these gains are about 50 V/V $(1 + R_5/R_3)$ and 200 V/V $(1 + R_{10}/R_8)$. The cut-off frequency (f_c) of 1.6 mHz is obtained using an AC filter. The filter consists of a thin film resistor (R_1 = 10 MΩ) and a stable metallized polyester capacitor (C_1 = 10μF, WIMA MKS2 type). The thermal noise of

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R_1 has a direct impact on the voltage noise. Below the cut-off frequency and for the impedance of the *device under test* (DUT) much lower than R_1, the amplifier input noise caused by the thermal noise of R_1 can be calculated:

$$v_{\mathrm{nR1}} = \sqrt{4kTR_1 \frac{f_c^2}{f^2}}, \tag{4}$$

where f is signal frequency and $f_c = 1/2\pi R_1 C_1$. The cut-off frequencies resulting from R_4C_2 and R_9C_4 components are about 2.4 mHz and 1 mHz, respectively. The stages are coupled using a R_6C_3 filter providing the cut-off frequency of 10 mHz. The determined frequency characteristics of this ULNA is presented in Fig. 6. Its signal bandwidth is from 20 mHz to around 600 kHz. For eight-paralleled transistors T_1, I_D was set to 34 mA by the values of both resistors R_2 and R_3 (5 W, wirewound). The voltage V_{DS} was 2.78 V. For transistor T_2, I_D was of 4 mA and V_{DS} = 3.6 V. The operating points allow to work in active (saturation) region of transistors' characteristics. This do not degrade noise performances caused by, *e.g.*, thermal fluctuations. Resistors R_3 and R_8 (wirewound) should have an optimally low resistance to obtain both low Johnson noise and high open loop gain ($R_3 < 1/g_m$). In the designed circuit, these values are of 10 Ω and 100 Ω, respectively. A_1 is a bipolar high-speed op amp (LT1028) with the ultra-low voltage noise of 0.85 nV$\sqrt{\text{Hz}}$ and 1 nV$\sqrt{\text{Hz}}$ for 1 kHz and 10 Hz, respectively. In the second stage A_2 of the amplifier, a JFET input op amp with the voltage noise of 3.3 nV$\sqrt{\text{Hz}}$ at 1 kHz and of 5.5 nV$\sqrt{\text{Hz}}$ at 10 Hz (ADA4625) is used.

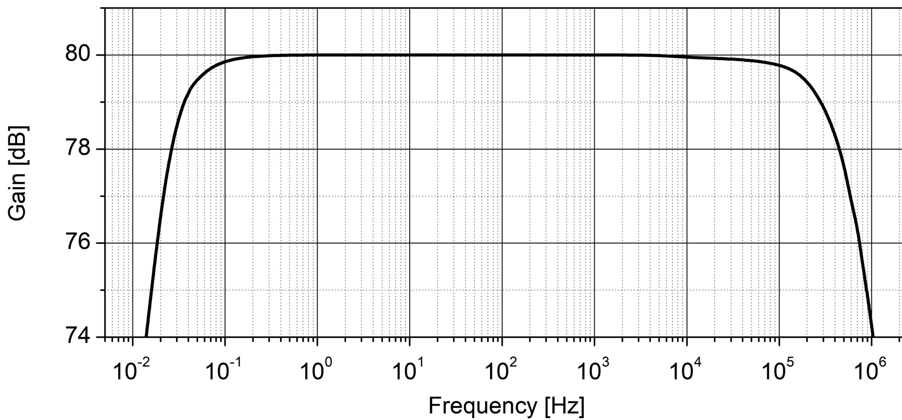

Fig. 6. ULNA frequency response.

A long time constant is the main disadvantage of this amplifier. To resolve this problem, extra switches can be implemented between the coupling capacitors' output and the ground. A special metal shielding case with isolated connectors for input and output signals is applied to reduce signals interferences.

The measurements of the output voltage noise were performed using a setup shown in Fig. 7. In the data acquisition process, an analogue anti-aliasing filter and a 16-bit A/D converter were used. This filter is constructed based on a Sallen–Key configuration with the cut-off frequency of 20 kHz. Signal samples were collected at the rate of 200 ksps.

The noise measurement of the designed ULNA was performed up to 1 kHz (Fig. 8). The $1/f$-noise frequency region is observed in the range of a few tenths of a Hz. Basing on both JFETs'

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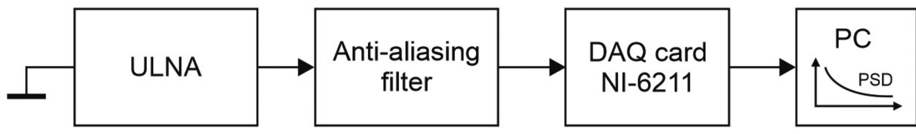

Fig. 7. Block diagram of noise measurement setup.

datasheets and the noise reduction factor of √8, the expected noise level was of around 3 nV/√Hz at 1 Hz, 0.71 nV/√Hz at 10 Hz, and 0.35 nV/√Hz at 100 Hz. During the measurements, the voltage noise was of ~3 nV/√Hz (1 Hz), 0.95 nV/√Hz (10 Hz) and 0.6 nV/√Hz (above 100 Hz). For the *1/f*-noise region, the results were similar. Some differences were observed in the white noise range. This could indicate the presence of additional sources of noise.

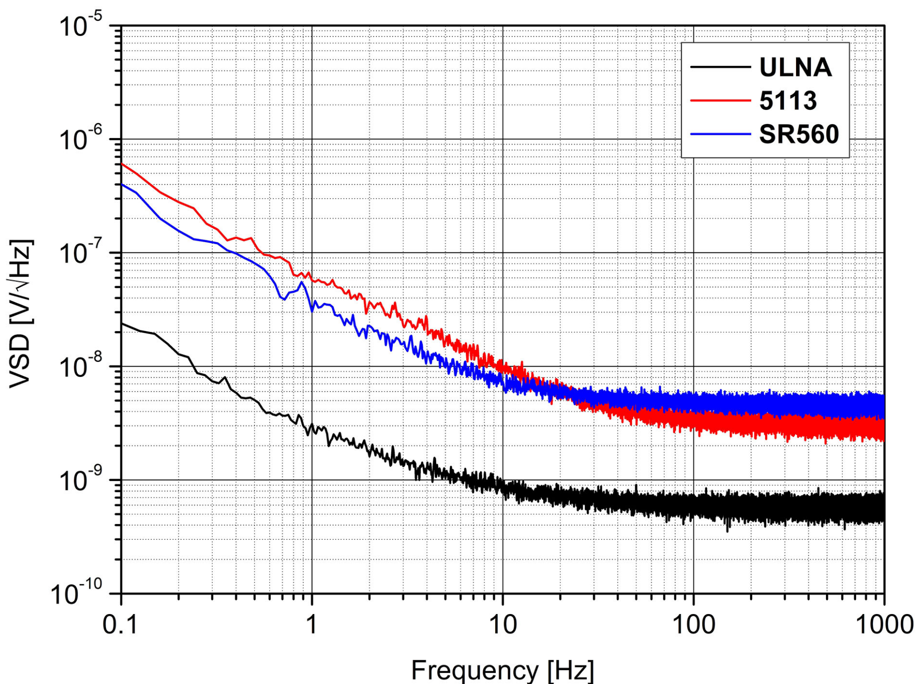

Fig. 8. Measured input voltage noise density vs. frequency for ULNA, 5113 and SR560 types.

To refer the obtained results, the voltage noise of two commercial voltage amplifiers (Stanford Research Systems SR560 and Signal Recovery Model 5113) was also measured. The amplifiers' signal inputs were grounded. Their gain was set to 5×10^3 ensuring reliable equivalent input voltage noise measurements. The catalogue noise data of these amplifiers are: 30 nV/√Hz (1 Hz), 6 nV/√Hz (10 Hz) and around 4 nV/√Hz (1 kHz) for an SR560 device and 4 nV/√Hz (1 kHz) for a Model 5113. There was noticed that the obtained results matched the catalogue ones. Any differences are probably caused by the no-defined production spread of the field-effect transistors' parameters. In the measured frequency range, the constructed ULNA has a much lower voltage noise than the tested commercial devices.

4. Summary

The paper presents a low noise voltage amplifier. It was built using some commonly-used JFET transistors. The obtained noise characteristics are lower in comparison with two commercial amplifiers (SR560 and 5113). Its construction is simple, but it offers the voltage noise of ~3 nV/√Hz (1 Hz), 0.95 nV/√Hz (10 Hz) and 0.6 nV/√Hz (above 100 Hz). However, it has also some disadvantages. There is a long setting time caused by high-pass filters with very low cut-off frequency. The amplifier has a constant gain of about 80 dB. However, very low voltage noise and FET input with high-pass filter allows to measure sources with AC coupling. The amplifier can be easily modified to obtain lower voltage noise (mainly at low frequencies from 0.1 Hz to 10 Hz). This modification consists in exchange input FET transistors (*e.g.*, lower noise model of IF9030 or IF3601) and in setting their operating point (V_{DS} and I_D).

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