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Diophantine equation based model of data transmission errors caused by interference generated by DC-DC converters with deterministic modulation

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Abstract. The assurance of the electromagnetic compatibility of sensitive smart metering systems and power electronic converters, which introduce high-level electromagnetic interference is important factor conditioning reliable operation of up to date power systems. Presented experimental results have shown that currently binding, frequency domain tests are ineffective for the evaluation of data transmission error hazards. The proposed in this paper mathematical, time-domain model, based on Diophantine equation, enables evaluation of data transmission errors caused by interference introduced by DC-DC power electronic interfaces with deterministic modulation. In the paper there have been presented possible application areas for the proposed model.

Key words: electromagnetic compatibility, electromagnetic interference, power electronic converters, Diophantine equation.

1. Introduction

Power electronic converters are increasingly being used as interfaces in Smart Grid systems [1–3], however due to pulse mode of operation and high *dv/dt* and *di/dt* rates they produce a substantial level of electromagnetic interference (EMI) [4–7], which is why power electronic converters are often treated by their designers as the main causes of industrial system malfunctions. Conducted EMI can be associated with unwanted currents and voltages that might be coupled, by means of parasitic couplings [8], to data transmission circuits. Superimposition of the EMI voltages onto voltages representing binary data signals may lead to data transmission errors.

Electro-Magnetic Compatibility (EMC), according to the European EMC Directive 2004/108/EC, "means the ability of equipment to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to other equipment in that environment". This general description requires detailed rules on how to evaluate EMC assurance. The evaluation is usually based on harmonization standards which provide strict measuring procedures. Fulfillment of the requirements of harmonization standards is taken as presumption of EMC compliance. However, the increasing number of novel power electronic interfaces generating a high level of electromagnetic interference (EMI), connected with susceptible control systems operating in time domain, has made currently binding frequency domain EMC standards obsolete.

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Thus, evaluation of the probability of the appearance of data transmission errors, caused by interference generated by power electronic converters, is important for both cognitive and technical reasons. Elaboration of the presented mathematical model has enabled explanation of significant differences in experimentally obtained distributions of awaiting times for data transmission errors caused by interference generated by a DC-DC converter with random [9–11] and deterministic modulation. The evaluated probability of the appearance of data transmission error may become a useful factor supporting the development of data transmission systems.

The DC-DC converter was selected as an interference source for mathematical analyses of data transmission errors caused by interference generated by converters with deterministic modulation. A detailed description of the interference introduced by a DC-DC converter [12–14] has been presented in our previous paper [15].

2. Deterministic vs. random modulation of power electronic interfaces

Random modulation of power electronic interfaces is often recommended as an EMI reduction technique [16, 17]. In fact the utilization of random modulation does provide ostensible reduction [18, 19] of the interference levels measured, in accordance with EMC standards, in the frequency domain. Fig. 1 shows the experimental results for conducted emission generated by a DC-DC converter with deterministic and random modulation, measured using average detector, in accordance with the EN 55022 standard, with the upper limit of the frequency range reduced from 30 MHz to 5 MHz for better clarity of the results.

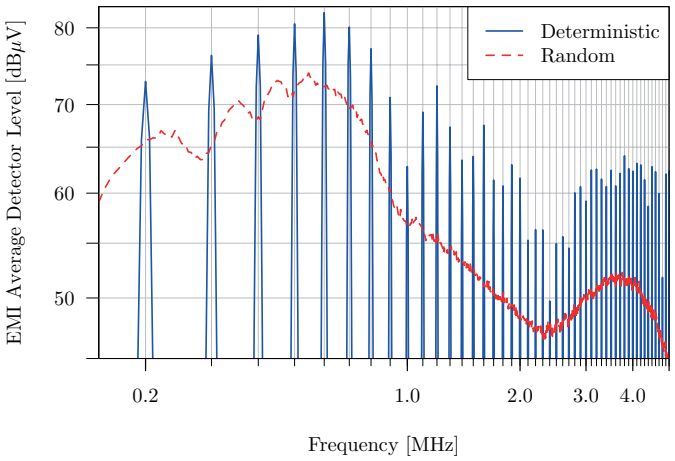

Fig. 1. Conducted electromagnetic interference, generated by deterministic and random modulated converters, measured according to EN 55022 standard, using average detector

In fact, a decrease in the observed interference levels has exceeded 6 dB. This means that the conducted emission, measured according to standards in the frequency domain, has been decreased more than twofold, without investment in converter hardware. However, commonly applied data transmission standards use time domain signals. Thus, the lowering of maximum levels of interference, caused by even distribution of interference over frequency range in the case of random modulation, does not imply lowering of interference waveforms in the time domain. The phenomenon of the appearance of interference caused by power electronic converters is precisely described in the literature [4, 20, 8]. The shape of the time-domain, damped oscillatory mode, interference pulse depends on the high frequency impedance of interference paths as well as rising and falling slopes of the converter voltages, exciting interference currents [4]. Thus, the waveform of the individual damped oscillatory mode pulse is identical in both the deterministic and the random modulation cases, only the moment of the its appearance is different. The typical experimental waveforms of the interference currents generated by a DC-DC converter with deterministic modulation are shown in Fig. 4.

3. Probability of the appearance of error caused by interference generated by DC-DC converters with deterministic and random modulation

In spite of the significant ostensible reduction in level of interference measured using normalized equipment our preliminary, experimental investigations have revealed that random modulation has no clear advantage over deterministic modulation in the context of data transmission errors induced by converter operation. Measurements have been made in a system consisting of a DC-DC power electronic converter with both deterministic and random modulation and a series data transmission system, representing distorted microprocessor control circuits, encountered in real situations. A comparison of distributions of awaiting times for data transmission errors caused by interference, generated by a DC-DC converter with random and deterministic modulation, has indicated significant dependence of the obtained results on the selected converter switching frequency. In order to evaluate this dependence, the time-consuming measurement of transmission errors for various converter switching frequencies have been performed. Figure 2 shows probabilities of data transmission error appearance caused by electromagnetic interference introduced by the same power electronic interface with both deterministic and random modulation for various converter switching frequencies (depicted by dots and squares). For each measuring point more than 1000 error events was collected for the probability evaluation.

The curves presented in Fig. 2 differ significantly, indicating the different natures of the phenomena of error appearing in the same system but with different modulation. Based on the presented data it is hard to say which modulation is better. In the case of the deterministic modulation small changes in switching frequency of the converter bring about significant differences in observed data transmission error probabilities. The obtained results encouraged the authors to make an in-depth investigation concerning descriptions of the phenomenon of data transmission error occurrence caused by DC-DC converters with deterministic modulation. The Diophantine equation-based model of data transmission errors caused by interference generated by DC-DC converters with deterministic modulation, as presented in this paper, constitutes a significant complement for the time-domain model of probability of data transmission error appearance in a system consisting of DC-DC converters with random modulation, as presented in our previous work [18].

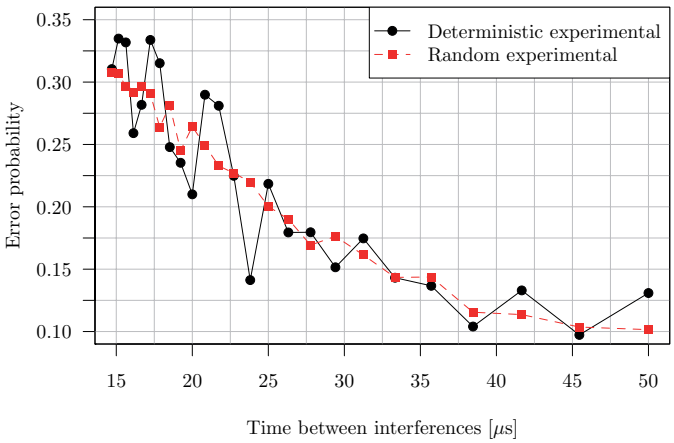

Fig. 2. Dependence between transmission error probability and time between interference pulses generated by deterministic and random modulated DC-DC converters

The aim of using the time-domain based model of data transmission to assess the probability of appearance of error in a system consisting of DC-DC converters with random modulation was to formulate a mathematical model based on the

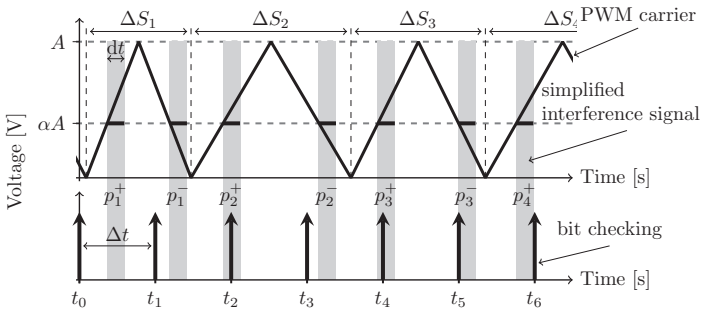

Fig. 3. Simplified scheme describing influence of the interference caused by DC-DC converter with random modulation on the transmission signal

knowledge of the occurrence of the phenomenon of data transmission error caused by interference introduced by PEIs. The model should be as simple as possible, yet should enable assessment of the probability of a transmission error occurrence during the transmission of a frame containing N-bits in the presence of interference with given parameters.

Figure 3 shows schematically the carrier function representing both deterministic ($\Delta S_i = \text{const}$) and random modulation ($\Delta S_i = \text{var}$) of PEI. The t_i depicts transmitted signal value checking moments while p_i^+ and p_i^- depict simplified interference signals introduced by operation of the converter.

Real interference signals are usually more complex than data signals, however measured interference signals can be simplified for the sake of the model [18]. In practice, the required parameters of the simplified interference signal can be determined on the basis of the time domain measurements of the interference voltage at the terminals of the transmission data receiver. The parameters of the simplified interference signals are depicted on the interference voltage waveform presented in Fig. 4.

The width dt of the simplified interference signals p_i^+ and p_i^- should be measured at a level that causes the appearance of error in a given transmission standard. In the investigated case the RS 232 transmission standard represents series transmission that is commonly used in microprocessor systems [18]. In the experimental arrangement the voltage levels from −3 V down to −5 V correspond to the binary "1" and levels from −3 V up to 5 V correspond to the binary "0", thus addition of the interference signals p_i^+, higher than 2 V, to the binary "1" and p_i^-, lower than 2 V, to the binary "0" brings about data transmission error.

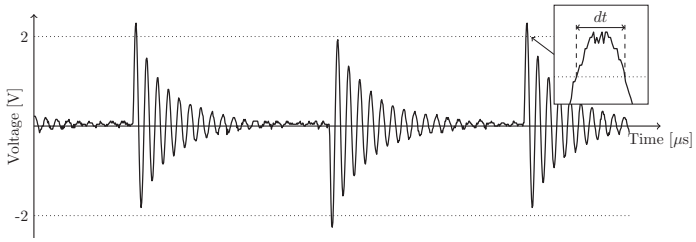

Fig. 4. Experimental waveform of interference voltage with depicted dt parameter of simplified interference signal

When the consecutive bits of information are sent in equal time intervals $\Delta t_i = \Delta t$ (const) and

$$0 < dt < \frac{1}{2} \min \{\Delta t,\ \Delta S_0\ (1 - \lambda)\}$$

then the probability of the appearance of error in N-bit frame can be expressed by [18]:

$$P_{\text{error}} = \sum_{k=0}^{N} \left(1 - (1 - p_e)^k\right) P(X = k), \tag{1}$$

where:

ΔS_0 – average period of the carrier function,

ΔS_i ($i = 1, 2, \ldots$) – are independent random variables of distributions $\mathscr{U}((1 - \lambda)\Delta S_0, (1 + \lambda)\Delta S_0)$, $\lambda \in (0, 1)$,

dt – is the established value representing the duration of the interference signal that can cause transmission error, depicted by a gray stripe,

p_i^+, p_i^- – points for $i = 1, 2, \ldots$ determine moments of "+" and "−" signal appearance, respectively,

n – number of bits in the transmitted frame,

t_i – moment of i-th bit sending.

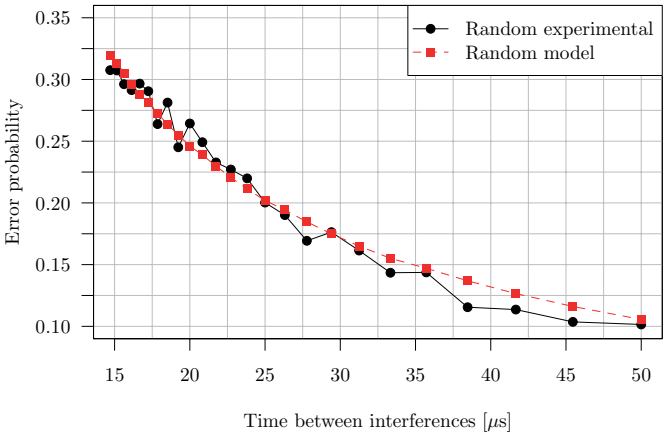

Fig. 5. Experimental and simulation dependencies between transmission error probability and time interval between interference pulses generated by random modulated DC-DC converters

Figure 5 shows the probabilities of the appearance of a data transmission error observed in the experimental arrangement with random modulation and corresponding probabilities evaluated on the basis of the probability of the appearance of a time-domain based model of data transmission error in a system consisting of DC-DC converters with random modulation, as presented in our previous work [18].

Both curves the experimentally obtained as well as the evaluated on the basis of the model fit well, however the model applicability is limited to random modulated converters. The limitation concerning minimum demanded level of ΔS_i variation is described in the paper [18].

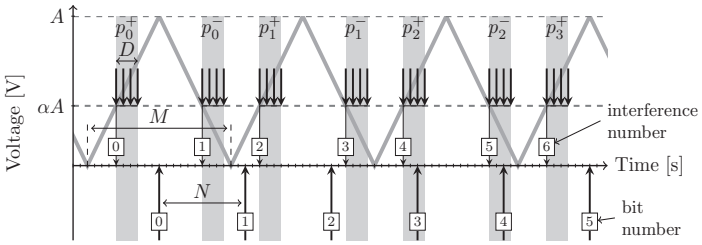

Fig. 6. Simplified scheme describing influence of the interference caused by DC-DC converter with deterministic modulation on the transmission signal

4. Diophantine equation based model of data transmission errors caused by interference generated by DC-DC converters with deterministic modulation

Figure 6 shows the scheme of data and interference signals constituting the basis for the Diophantine equation based model of data transmission errors caused by interference generated by DC-DC converters with deterministic modulation. The scheme was elaborated on the basis of the physical knowledge about the phenomenon of the interference generation by DC-DC converters with deterministic modulation and the occurrence of errors induced by interference of given parameters [15, 19].

4.1 Time discretization. In order to apply the Diophantine equation, the time has been discretized with the step τ. For deterministic modulation the triangle carrier function has a fixed period, thus $\Delta S_i = \Delta S_0 = \text{const}$, for $i = 1, 2, \ldots$, moreover, it could be assumed that for some $M, N, D \in \mathbb{N}$ there is a relationship

$$\Delta S_0 = M\tau, \quad \Delta t = N\tau, \quad dt = (D-1)\tau, \quad \alpha M \in \mathbb{N}.$$

Then M determines the interval between the interference pulses, N the time between bit value checking moments, D the distretized time of the simplified interference pulse, as shown in Fig. 6.

4.2. Data signal model assumptions. The n bits of information are transmitted in N discrete time intervals. There is no lack of generality if we assume that zero bit of information is sent in the 0 moment. Therefore, the moment of the j-th bit appearance is expressed by:

$$Nj, \quad j = 0, \ldots, n-1. \tag{2}$$

4.3. Interference signal model assumptions. In practice bit checking time is much shorter than the duration of the interference signal, which can cause transmission error. The bit checking time is the time required for determination of the voltage level that is connected with "0" or "1" bit representation. Interference signals appear in time intervals M and the width of the single, simplified signal is equal to D of discrete time intervals. Without the lack of generality, it can be assumed that the zero interference signal appears not later than zero data signal. Generally, it can be written that d-th discrete time interval of i-th interference signal appears in moment:

$$\begin{aligned} &M((1-\alpha)(i \bmod 2) + (\mathrm{i} \operatorname{div} 2)) + t + d, \\ &i = 0, 1, \ldots, t = 1-M, 2-M, \ldots, 0, d = 0, 1, \ldots, D-1, \end{aligned} \tag{3}$$

where t is the moment of the appearance of the zero interference signal.

4.4. Superimposition of data and interference signals. The interference signal is superimposed on the bit-checking moment, when the equation, with earlier assumed conditions, is satisfied:

$$Nj - M((1-\alpha)(i \bmod 2) + (\mathrm{i} \operatorname{div} 2)) - t - d = 0, \tag{4}$$

with conditions

$$\begin{aligned} &i \in \mathbb{N},\ j \in \{0, 1, \ldots,\ n-1\}, \\ &t \in \{1-M, 2-M, \ldots, 0\},\ d \in \{0, 1, \ldots, D-1\}, \end{aligned} \tag{5}$$

and known $N, M \in \mathbb{N}, \alpha(\alpha M \in \mathbb{N})$.

The equation 4 is known as Diophantine equation [21–24].

4.5. Estimation of the probability of the appearance of a data transmission error caused by interference generated by DC-DC converters with deterministic modulation using Diophantine equation-based model. In order to validate an applicability of the proposed Diophantine equation-based model the calculations corresponding to experimentally obtained results presented in Fig. 2 have been performed. An estimation of the probability of the appearance of a data transmission error caused by interference introduced by DC-DC converters with deterministic modulation requires the assumptions presented below.

Theorem 1. The quadruples (j, d, t, i) satisfying the Diophantine equation (4) are given parametrically by

$$\begin{aligned} t &= (Nj \bmod (-\mathrm{M}) - \mathrm{d} - (1-\alpha)\mathrm{Mk})) \bmod (-\mathrm{M}), \\ i &= 2\frac{Nj - t - d - (1-\alpha)Mk}{M} + k, \end{aligned} \tag{6}$$

where $j = \in \{0, 1, \ldots, n-1\}$, $d \in \{0, 1, \ldots, D-1\}$ and $k \in \{0, 1\}$.

Proof. By substitution of (6) into (4).

In the further investigation, there will be analyzed the number of information bits disturbed by interference signals, for the assumed condition that the 0-bit of information will emerge at moment t_0.

Definition 1. Let

$$L(t_0) = \#\{(j, d, t, i) : t = t_0\}, \tag{7}$$

where (j, d, t, i) satisfying (4).

Unfortunately, except specific cases in which N and M are co-prime numbers, there is no general formula for function $L(t_0)$. Thus, a numerical evaluation must be performed.

According to the above mentioned assumptions both the data and interference signals are deterministic, but the moment of the appearance of the interference signal is random. Let's assume that t is discrete uniform distribution with the interval $[1-M, 0]$, then the probability of the appearance of data transmission error (using the Theorem of Total Probability [25]), caused by interference signal introduced by a DC-DC converter with deterministic modulation, is equal to:

$$P(error) = \frac{1}{M}\sum_{t_0=1-M}^{0} 1-\left(\frac{1}{2}\right)^{L(t_0)} = \\ = 1-\frac{1}{M}\sum_{t_0=1-M}^{0}\left(\frac{1}{2}\right)^{L(t_0)}. \tag{8}$$

Note that the probability of the appearance of error in transmitted data is the arithmetic mean of the probabilities of error occurrence for a specified period of the appearance of interference signal. The numerical analyses were performed using R software environment for statistical computing and graphics [26].

Figure 7 shows the probabilities of the appearance of data transmission error for different converter switching frequencies. The solid curve shows probabilities calculated on the basis of the experimental results, while the dashed curve depicts probabilities evaluated using the proposed model. Observed differences between the presented curves result from inaccuracy of the parameters of the DC-DC converter and data transmission system. However, despite inherent inaccuracy of the experimentally determined parameters, measured in a real arrangement, the Diophantine equation-based model is still capable of predicting the probability of error to a satisfactory level of accuracy.

Moreover, the performed analyses, using the proposed model, have enabled the authors to understand the physical and mathematical reasons for significant differences observed in error probabilities for small changes of converter switching frequency, presented in Fig. 2. In has been revealed that these unexpected differences result directly from the divisibility of numbers. The higher the smallest common divisor of time between bit checking moments (N) and the time between interferences (M), the smaller the error probability is.

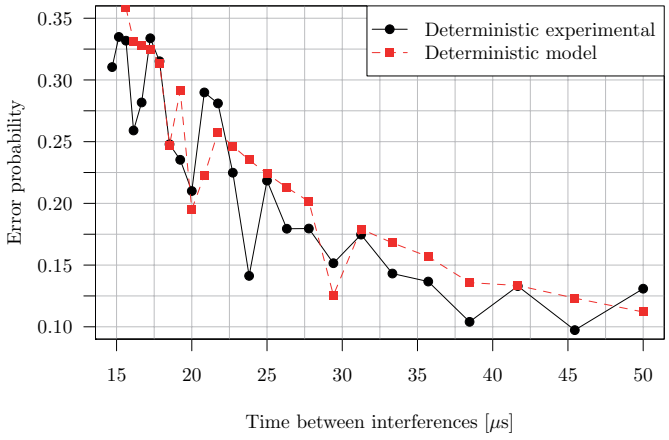

Fig. 7. Experimental and simulation dependencies between transmission error probability and time between interference pulses generated by DC-DC converters with deterministic modulation

In-depth understanding of the side-effect phenomena, accompanying the application of new technologies, usually enables development and application of low cost mitigating techniques. The proposed model for the appearance of error caused by interference, generated by a converter with deterministic modulation, might be directly used by practitioners. In the case of the observed high probability of the appearance of error, resulting in significant decreasing of the data transfer rate, the switching frequency of the locally installed converters with deterministic modulation should be slightly changed. Producers of converters with deterministic modulation might offer such fixture without investments in hardware.

5. Conclusion

The proposed Diophantine equation-based model of the probability of the appearance of transmission error caused by interference generated by DC-DC converters constitutes a significant complement for a time-domain based model of the probability of the appearance of data transmission error in system consisting of DC-DC converters with random modulation, as presented in our previous work. The mathematical model explains significant differences between probabilities of data transmission errors caused by interferences generated by deterministic and random modulated converters, observed in experimentally obtained results. It has been revealed that the probability of the appearance of transmission error in systems with deterministic modulated converters depends on the smallest common divisor of time between bit-checking moments and the time between interferences. Besides cognitive value, the presented model, based on the Diophantine equation and physical knowledge about interference induced transmission errors, can be used in engineering practice. The model can be applied in order to:

- determine probability of transmission error appearance in real situation, based on experimental waveforms,
- make a decision about investments in EMI reduction techniques, assuring reliable data transmission,
- increase the data transfer rate by small changes of the converter switching frequency,
- elaborate new, time-domain based, EMC standards, etc.

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