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Sampler – Open-Source Data Acquisition Module for Quantum Physics

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***Abstract*—The Sinara hardware platform is a modular, open-source measurement and control system dedicated to quantum applications that require hard real-time performance. The hardware is controlled and managed by the ARTIQ, open-source software that provides nanosecond timing resolution and sub-microsecond latency. The Sampler is a general-purpose precision ADC sampling unit with programmable gain and configurable interface. It is used in numerous applications like laser frequency and intensity servo. This paper presents the Sampler module construction and obtained characteristics.**

***Keywords*—ADC; FPGA; ion trap; ARTIQ; Sinara; quantum instrumentation**

I. Introduction

Control electronics used in many trapped-ion and other quantum physics experiments suffer from several problems. In general, an improvised solution is built in-house without enough consideration about good design, reproducibility, testing, and documentation. It makes those systems unreliable, fragile, and difficult to use, maintain, and reproduce in other labs. It also duplicates work in different laboratories. Also, the performance and features of the existing systems (e.g. regarding pulse shaping abilities) are becoming insufficient for some experiments.

Sinara and ARTIQ[1] projects address the above issues by providing a crowd-funded, collaborative hardware and software environment that is both open-source and commercially available [2][3]. The community involved in the Sinara project successfully developed over 40 boards and modules for three years. Most of them are available commercially. Sampler module[4] is, apart from Kasli FPGA controller[5], one of the most used building blocks of many control systems built with Sinara ecosystem. An example control system built with Sinara hardware is shown in Fig. 1.

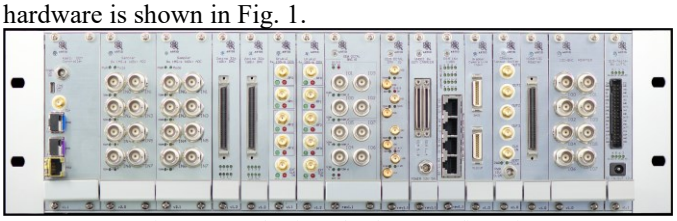

Fig. 1. Example Sinara hardware configuration

II. Sampler Module

The Sampler (Fig. 2) is an 8-channel, 16-bit ADC EEM[6] with an update rate of up to 1.5MSPS (all channels simultaneously). It has a low-noise differential front end with a digitally programmable gain, providing full-scale input ranges between +-10mV (G=1000) and +-10V (G=1).

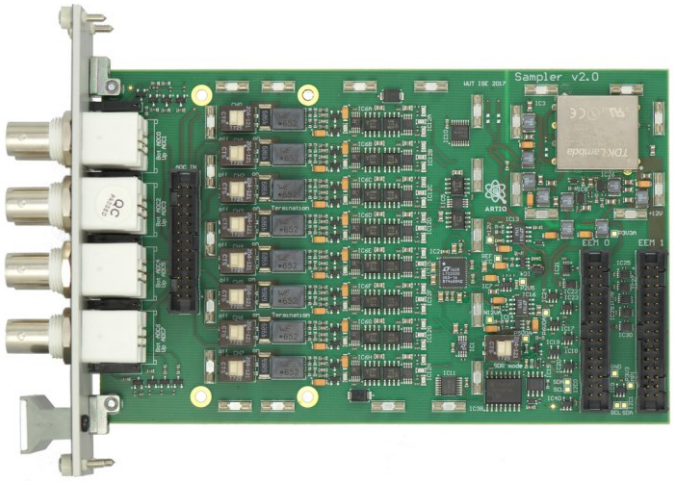

Fig. 2. Sampler module rev.2.0

Complete project documentation, including the source schematics, PCB layout, as well as production files is available from the Github repository [7]. Project sources were published under the CERN OHL license. The module parameters are listed in Table I.

III. Block Schematic and Design Considerations

The Sampler module block schematic is presented in Fig. 1. Due to the limited number of LVDS links, the SPI extender was used to control the gain of individual channels. One of the most critical requirements for the Sampler module was the low-temperature coefficient, better than 5ppm. For this reason, all the critical components must meet strict requirements. All gain setting resistors were implemented as matched 5ppm resistor arrays from Vishay. All references for both ADC and driver were generated from a common 2ppm 4.096V source using low-temperature co-matched resistors from Vishay (Fig. 6). The

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resistors were connected in series and parallel way to limit the number of BOM positions.

The analog front end is a critical block of every data acquisition system. Quantum labs are usually densely packed with sophisticated equipment which also makes ground loop management difficult. The Sampler module AFE (Fig. 7) was designed to mitigate ground loop issues. The BNC connectors can have their external contact floating. Such an approach makes the input as fully differential, breaking the ground loop.

TABLE I
MODULE FEATURES

Parameter	Value
Module width	4HP (MCX connectors) or 8HP(BNC connectors)
Channel count	8
Resolution	16-bit
Sample rate	up to 1.5 MHz per channel
Sustained aggregate data rate in single-EEM mode	(8 channel readout): ~700 kHz
Sustained per-channel data rate in dual-EEM mode	(8 channel readout): ~1MHz
Current hardware revision	2.2
-6dB bandwidth[a]	200kHz for G={1, 10, 100} 90kHz for G=1000
Input ranges	+-10V (G=1) +-1V (G=10) +-100mV (G=100) +-10mV (G=1000)
DC input impedance	Termination off: 100k Termination on: 50Ohm
Chipset	ADC: LTC2320-16 PGIA: AD8253
Power consumption	Max 4.1W

[a] The bandwidth specifications on this page are for the hardware only; ARTIQ kernel and RTIO overhead often make the effective sample rate lower

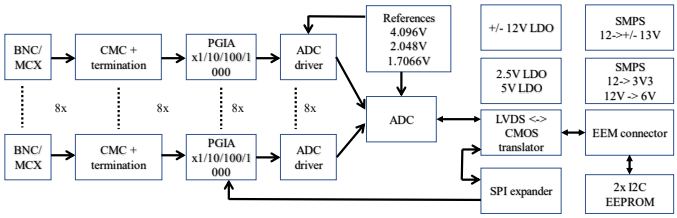

Fig. 3. Sampler block schematic

To increase the common-mode rejection ratio, especially for higher frequencies, the Common Mode Choke (CMC) was added. It forms a low pass filter for common signals. The cutout frequency was chosen to be lower than the instrumentation gain amplifier CMRR cutoff frequency. CMRR of the AFE with and without the CMC is presented in Fig. 4 and Fig. 5.

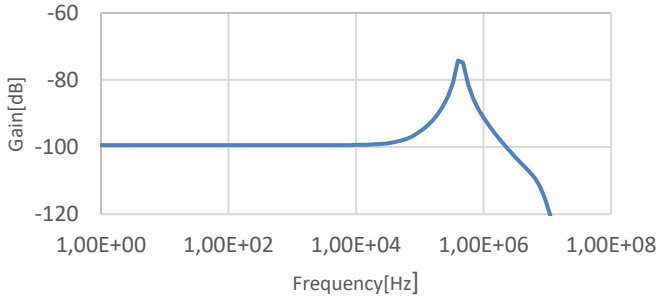

Fig. 4. The Sampler channel CMRR TinaTI simulation with the common mode choke

In order to support +/- 10V operation, the AFE must be supplied from +/-12V supplies. Care was taken during the design of the power supply chain. The +/-13V SMPS module was used, followed by 4th order LC filter and high PSRR LDO. High-ESR tantalum capacitors were used to damp LC filter oscillations (Fig. 8). A power sequencing circuit was added to make sure that AFE gets supplied after the ADC to avoid latch-up and IC damage.

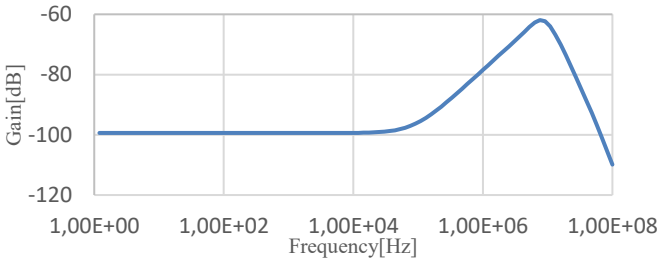

Fig. 5. The Sampler channel CMRR TinaTI simulation without the common mode choke

The Sampler module is connected with the FPGA controller using the 8 or 16 - channel LVDS interface. To properly identify the module version and interface configuration (single or double EEM), each EEM interface has a dedicated I2C interface connected to an EEPROM with a unique ID. The EEPROM holds a record with module identification string, HW version, manufacturer, date, etc. Such an approach makes firmware development much easier since the software driver can check if it is compatible with installed hardware module.

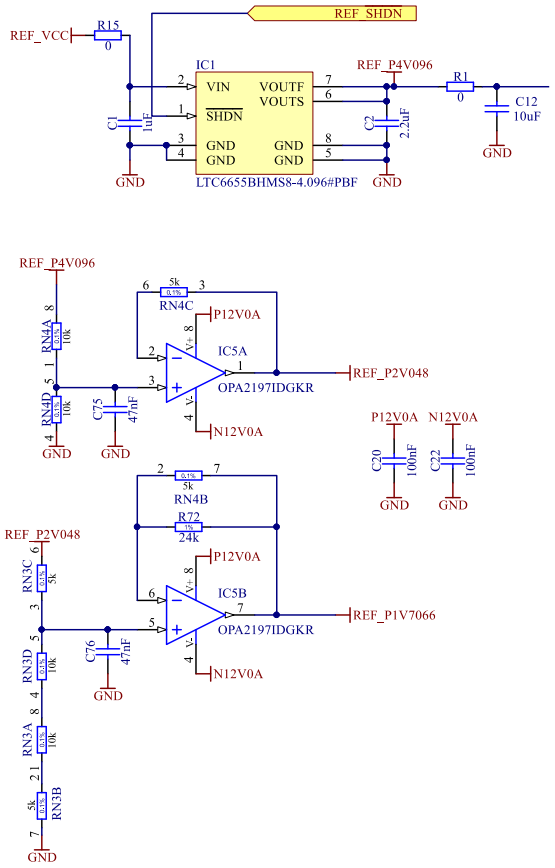

Fig. 6. Reference source

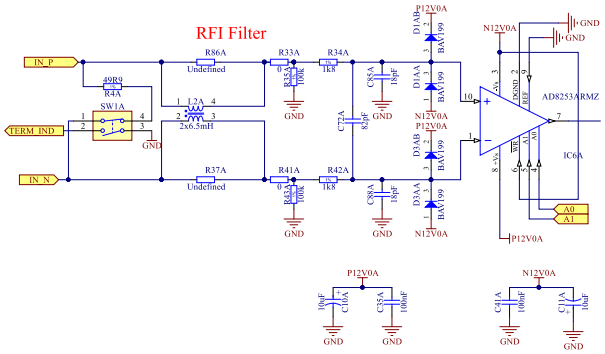

Fig. 7. Analog Front End

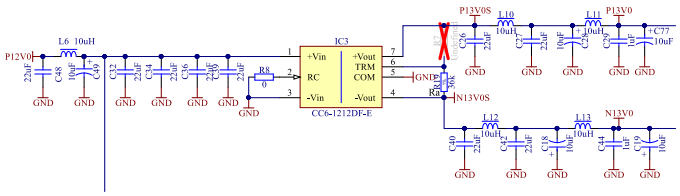

Fig. 8. AFE block power supply and filter (LDOs were not shown)

IV. Modes of Operation

Sampler module can be operated either in a basic mode as a standard SPI EEM using a single EEM connector (EEM0), or in fast mode via a source-synchronous LVDS interface and 2 EEM connectors (EEM0-EEM1). In basic mode, the channels must be read out sequentially in decreasing order. The maximum SPI clock is limited by the round-trip delay in the cabling used to connect Sampler to the master FPGA controller. With a 20 MHz SPI read clock (25ns round trip plus setup), we get one sample for each channel per 6.9us.

Fast mode allows all ADC channels to be read out simultaneously at 1.5 MHz via a source-synchronous interface. This is implemented (~ 1 MHz on each channel for all channels) in the Kasli-Sampler-Urukul laser intensity servo[8].

The Sampler can operate with externally applied signals through the BNC connectors. It can also operate with custom-made Analog Front End mezzanines installed on top of the Sampler module. Signals are then routed via a dedicated IDC connector. It further extends the functionality of the module.

V. Assembly Variants

The Sampler can be assembled with BNC or MCX connectors. BNC version (Fig. 10) is a default configuration, and it requires 8 HP front panel. The module can also be assembled with MCX connectors and 4HP front panel. It is achieved using a simple MCX adapter board (Fig. 9). Such configuration is required in a high-density multi-channel system as well as in compatibility mode with CERN DI/OT system[9].

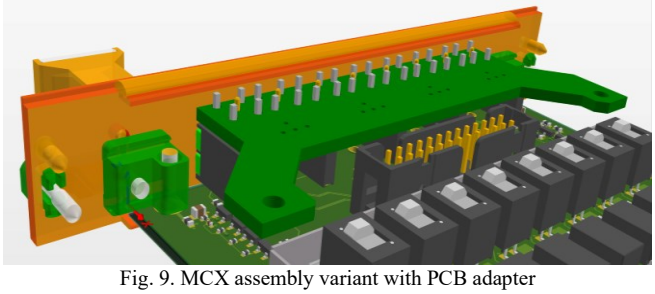

Fig. 9. MCX assembly variant with PCB adapter

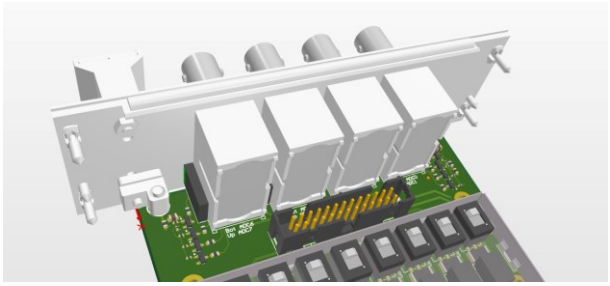

Fig. 10. Assembly variant with BNC connectors

VI. CERN DI/OT Compatibility Mode

CERN develops its instrumentation standard for accelerator control and diagnostics, based on CompactPCI Serial[10][11]. Since Sinara also uses a 3U Eurocard standard and very similar LVDS connectivity, an adapter that ensures compatibility with DI/OT system was designed. The adapter[12] ensures both mechanical and electrical interface between CompactPCI Serial backplane and EEM boards(Fig. 11, Fig. 12). For a configuration with CPCIS backplane, the original DI/OT controller based on ZynQ US+, developed by CERN will be used. The existing Kasli controller will also be equipped with a suitable adapter. The backplane apart from LVDS, I2C, and power connectivity provides also the distribution of low jitter DRTIO[13] clock signal.

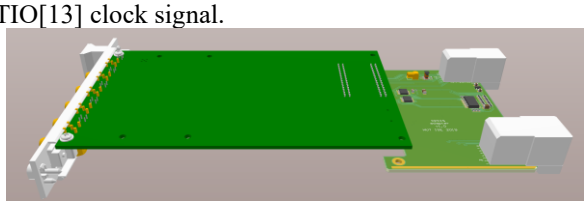

Fig. 11. Sampler EEM module with CompactPCI Serial adapter

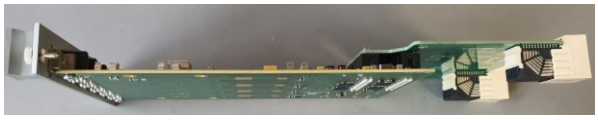

Fig. 12 Side view of the EEM mocule with CompactPCI Serial adapter

Such a combo construction will be covered by a double-sided metal shell that will increase its stiffness and protect it against mechanical damage, especially components assembled on the bottom side of the PCB(Fig. 13).

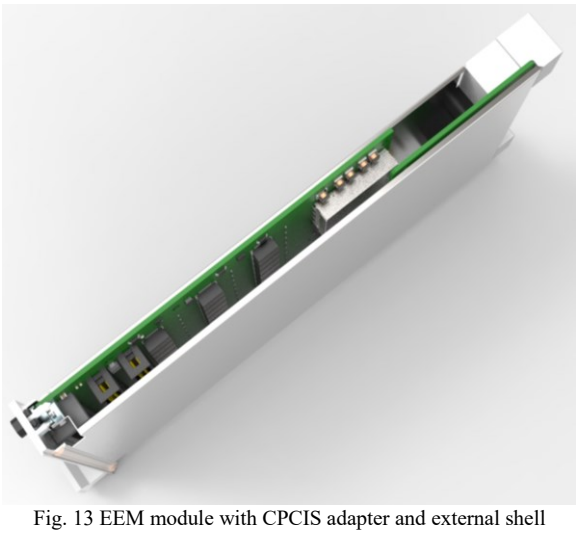

Fig. 13 EEM module with CPCIS adapter and external shell

VII. Design Verification

The design was verified before production. All critical blocks were verified with SPICE simulations before drawing the schematics. Since ground loop mitigation is essential for module operation, special care was taken during AFE design. Fig. 4 and Fig. 5 present AFE CMRR characteristics with and without common mode choke. One can easily notice the difference and poor instrumentation amplifier performance above the 100kHz without the common mode choke.

After PCB layout and routing, the design was validated in terms of Signal Integrity and Power Integrity using the Mentor Graphics Hyperlynx tool. Voltage drop and current density analysis for +12V AFE rail are presented in Fig. 14.

Very rigorous tests in various scenarios were performed. Unless stated otherwise, all measurements use: 200kHz ADC clock, input termination off for signals connected directly to a voltage source, termination on for "floating" inputs, gain =1. The module was also tested and is currently working in numerous experiments, mainly related to ion traps.

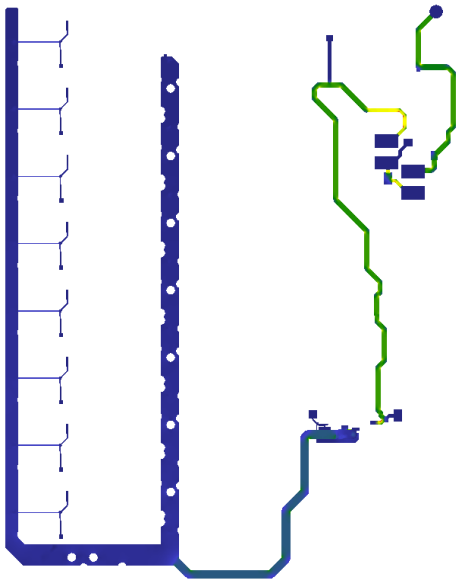

Fig. 14. 12V AFE rail current density

VIII. Tests and Characterisation

A. Bandwidth

An input (termination off) was driven from a signal generator. Scan the signal frequency to measure the -6dB frequency on the ADC. The sample rate was 125kSPS, so the signal frequency was above the Nyquist frequency for most gain settings.

B. Small-signal bandwidth

Signal was nominally sinus 2Vpp/Gain driven by Keysight 33500B generator. The characteristics are presented in Fig. 15, the measurements are presented in Table VI.

C. Large-signal bandwidth

We made the following measurements, which confirm that the large-signal bandwidth is the same as the small-signal bandwidth to within the measurement accuracy for gains of 1 and 10. Large-signal bandwidth was measured using 15Vpp/Gain. The characteristics are presented in Fig. 16.

D. Noise floor

The sample rate for this measurement was 83kHz; the measurement bin width was 10k samples, averaged over 100 measurements. Channel 6 had the 50R termination on, 7 had the termination off. We were looking at the ADC noise as a function of frequency for different gains (Fig. 17, Fig. 18). The results are presented in Table II.

Spurs are most likely due to the pickup noise. Adding/removing the two screening cans doesn't make a noticeable difference to the data. Running from a linear PSU/wall wart doesn't make a difference, nor does connect the linear PSU output to GND.

E. Channel-channel cross-talk

For DC cross-talk measurement the input A was connected to +-17V DC, termination was off. This voltage is clipped by the protection diodes but was chosen to stress-test the design. The Input B with termination on was used to measure the signal level. With input B G=1, the voltage applied to input A makes <1LSB change in level measured at input B. DC cross-talk is thus < -96dB.

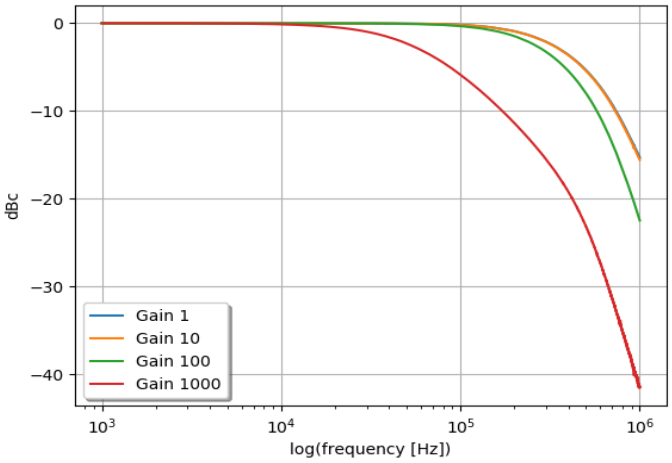

Fig. 15.Small signal bandwidth

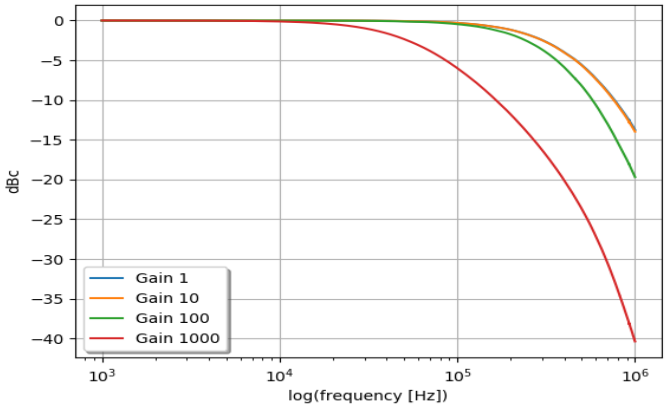

Fig. 16. Large signal bandwidth

TABLE VI
SMALL SIGNAL BANDWIDTH MEASUREMENT RESULTS

Gain	-6dB bandwidth
1	206kHz
10	207kHz
100	195kHz
1000	87kHz

TABLE II
NOISE MEASUREMENT RESULTS

Gain	Noise with termination	Noise without termination
1	1.78LSB (544.3uV)	1.75LSB (535.6uV)
10	1.84LSB (56.2uV)	3.09LSB (94.4uV)
100	3.47LSB (10.6uV)	26.02LSB (79.4uV)
1000	13.87LSB (4.2uV)	206.3LSB (63.0uV)

For AC cross-talk measurement the gain was the same on all channels. We applied the 50kHz, 10Vpp (-8.8dBFS) signal to one channel. The signal was measured on the adjacent channel as a function of PGIA gain. The termination was on for the driven channel, but off for all other channels. Note that the lack of dependence of the cross-talk on PGIA gain suggests that the cross-talk is dominated by pickup before the PGIA, most-likely in the BNC connector. The results are presented in Table III.

F. *Common-mode rejection ratio (CMMR)*

The input contact was shorted with a shield for one channel. A sinewave signal was applied to the input signal/ground. We measured the signal level seen by the ADC. The results are presented in Table IV for G=1 and table V for G=100.

G. *Harmonics*

Methodology: 25kHz signal applied to the input. The level of the second harmonic (50kHz) was measured as a function of the input signal level. The results are presented in Table VI.

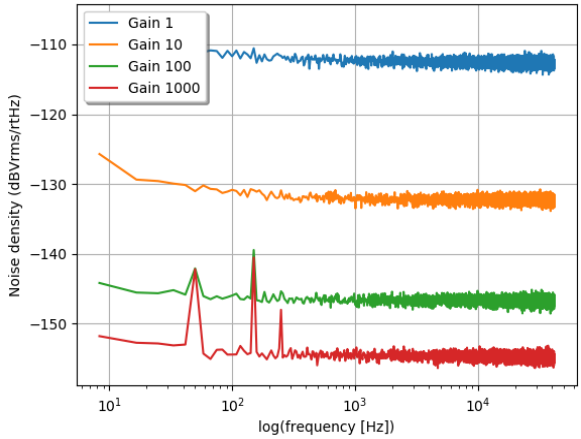

Fig. 17. Noise density for ADC channel with 50Ohm termination

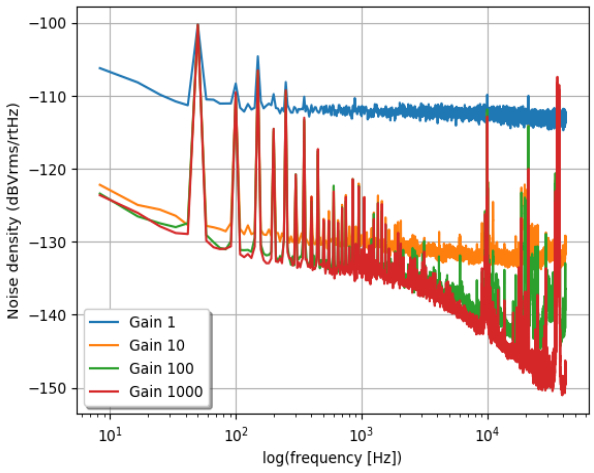

Fig. 18. Noise density for ADC channel without termination

TABLE III
CROSSTALK MEASUREMENT RESULTS

Gain	Signal	Crosstalk
1	-87dBFS	-79.2dBc
10	-67dBFS	-78.2dBc
100	-46dBFS	-77.2dBc
1000	-29dBFS	-81.2dBc

More measurements and results are available on the project Wiki page[4].

TABLE IV
COMMON MODE MEASUREMENT RESULTS FOR G=1

Frequency [kHz]	Measured signal level	CMRR [dB]
0.01	<-120	>-98
0.1	< -120	>-98
1	<-120	>-98
10	-109	- 87
100	-87	-55
1000	-105	-83
10000	-108	-85

TABLE V
COMMON MODE MEASUREMENT RESULTS FOR G=100

Frequency [kHz]	Measured signal level	CMRR [dB]
0.01	<-110	>-118
0.1	-98	-116
1	-88	- 106
10	-70	- 88
100	-50	- 68
1000	-80	- 98
10000	<-100	>-118

TABLE VI
HARMONICS MEASUREMENT RESULTS

Input level	Second Harmonic
0.1Vpp (-48dBFs)	-51dBc
1Vpp (-28dBFs)	-69dBc
10Vpp (-8dBFs)	-58.8dBc

IX. SOFTWARE

The Sampler module is fully supported by ARTIQ operating system. The ARTIQ (Advanced Real-Time Infrastructure for Quantum physics) is a leading-edge control system for quantum information experiments. It was initiated and developed in partnership with the Ion Storage Group at NIST and is now used and supported by a growing number of research institutions worldwide. While ARTIQ is currently mostly used by atomic physics groups, its applicability reaches beyond the ion trapping.

ARTIQ features a high-level programming language, based on Python, that helps to describe complex experiments. It is compiled and executed on dedicated FPGA hardware (for example Kasli controller) with nanosecond timing resolution and sub-microsecond latency. The time-critical code (a kernel) running on the FPGA (the core device) is easily interfaced with a Python code on the computer using a remote procedure call (RPC) mechanism. The FPGA design is highly portable so that it can adapt to different laboratory setups and resist hardware obsolescence. The ARTIQ drivers for non-real-time devices can be run on remote machines with different operating systems. The project also includes a graphical user interface, an experiment scheduling system, and databases for experiments, devices, parameters, and results.

The integration of the ADC module with the rest of the system is very simple and can be implemented by just a few lines of code. Example Python code of the laser intensity servo can be found on Github[14].

X. System Tests and Applications

The module was produced in tens of pieces and is currently installed in numerous experiments, mainly in the UK, US, DE, and China. Fig. 19 presents an example application of the Sampler module in the quantum experiment. The setup is the multi-channel laser intensity servo, where Sampler acquires the photodiode signal. Sampled data are fed to the IIR filter and the algorithm implemented in the FPGA controller (Kasli)[15] which steers the four-channel DDS module (Urukul)[16] and eight-channel power amplifier (Booster)[17]. During the debugging phase over 20 issues were found and fixed resulting in 4 hardware revisions. It is currently considered as a stable and mature product and an example of a successful approach to the open-source collaboration in instrumentation for quantum physics.

The Sampler module concept was proposed by the community on 17th February 2017. The latest release 2.2 was published on 27th July 2018. It took roughly 18 months to develop, test and fully characterize the product.

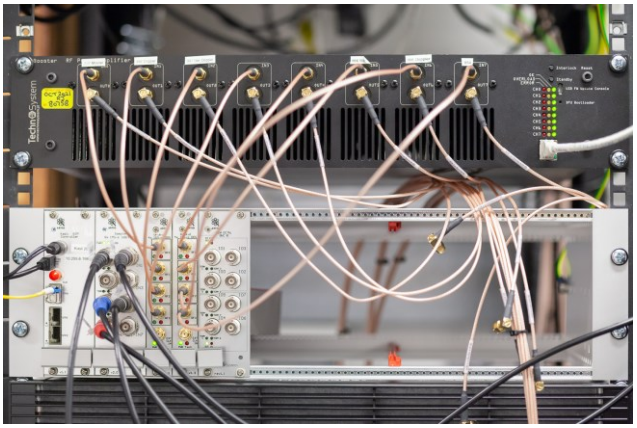

Fig. 19. Experimental setup with Sampler module as a part of multi-channel laser intensity servo

Conclusions

The most important parameters of the system, which differentiate its performance from any other one available on the market are:

- Modular form factor that enables scalability of the system to thousands of channels thanks to the DRTIO protocol
- Very low latency due to lack of higher-order communication protocol
- Two assembly variants, for high-density MCX and popular BNC connectivity option. Such approach fits both industrial and experimental applications
- Open source design, including hardware and software that makes it attractive to the user because it mitigates product life cycle and support issues
- Support for low-cost application with simple 3U Eurocard rack, convection cooling and IDC cables connectivity as well as professional applications. The second make use of CompactPCI Serial rack with power and temperature management, rugged mechanics and provides EMC compliance
- Good fit for particular applications in experimental quantum physics. The design was created using bottom-up approach where the end-users defined requirements and cooperated together on all stages of research and resign as well as production and testing phases. Popular COTS products are designed for general industrial use, so do not take into account specific client needs.
- Support for ARTIQ operating system. Building hard-real-time applications with Sinara modules in may cases can be done with just a few lines of Python code.
- Two commercial vendors support same Sinara products. Such approach is essential to the success of open-source product because gives the end-used comfort of switching to another vendor without a need of doing any modification in the setup. An example of very successful open-source application with commercial success is White Rabbit Switch[18]. Sinara follows the same approach.

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