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GaN-based soft-switched active power buffer operating at ZCS – problems of start-up and shut-down

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Abstract. This paper describes practical issues related to control of the active power buffer (APB) developed for a 2 kVA single-phase inverter. The buffer is designed using the latest GaN HEMTs controlled with triangular current mode to reduce switching losses, however, the switching frequency should be limited to 1 MHz. In the case of the presented analogue-digital controller, frequency is influenced by a reference current of the APB and circuit. Therefore, the operation at start-up and shut-down is especially challenging. A modified control algorithm that also includes pre-charging and discharging process of the energy buffer is presented and experimentally verified by series of tests of the 2 kVA GaN based inverter with the APB.

Key words: GaN, power inverter, active buffer.

1. Introduction

Recently GaN transistors, mainly based on High Electron Mobility Transistor (HEMT) structure, are considered as a device of choice when power switches for low-power single phase inverters are investigated [1, 2]. In comparison to superjunction silicon MOSFETs, but also relatively novel SiC MOSFETs [3], GaN HEMTs show much lower gate charge and, in consequence, better switching performance [4, 5]. Thus, switching frequency of the hard-switching inverters in the power range up to 5 kVA may be elevated much above 100 kHz [1, 2, 6]. The clear benefit from such a rise of switching frequency is a significant decrease of the output filter parameters – both inductors and capacitors become much lighter. Unfortunately, high switching frequency does not affect DC-side capacitor, which must be rated in relation to output current to limit power pulsation caused by the second harmonic component of the inverter current. Therefore, the increase of the power density introduced by GaN transistors meets an obstacle in miniaturization due to a bank of bulky electrolytic capacitors with well known disadvantages [6].

A possible solution here is an application of additional circuit to compensate a negative impact of the second harmonic component [7–10], usually named as active power buffer (APB), which may be also based on GaN HEMTs [11]. Results of Google Little Box Challenge proved that only designs with active power buffers and wide bandgap semiconductors offered serious increase of power densities [12]. A concept of additional electronic circuit has been investigated in different configurations for Si transistors [7]. An introduction of faster wide bandgap devices has resulted in further reduction of active power buffers, especially when additional techniques such as zero current switching (ZCS) are applied [11]. In consequence, size of the DC side capacitor may be significantly reduced as power pulsations are compensated by power buffer with very limited volume and weight. On the other hand, various challenges regarding capacitors have been studied recently [13–15] to find optimal solution for energy storage.

The main advantage of the electrolytic DC side capacitor is a permanent availability in the circuit, which means that power pulsations are always under control. This may be a challenge for active power buffer as safe operation requires specific conditions, to mention only suitable amount of energy stored in the capacitive buffer. Therefore, in addition to basic role, like compensation, of the power pulsations, behaviour of the active power buffer during system start-up and shut-down should be investigated. Recent works [16, 17], in addition to previous essential papers [7, 11] focus on steady state operation or pulse response only. Therefore, the main aspect of this paper describing a general problem of 2nd harmonic compensation in Section 2 as well as 2 kVA GaN based inverter in Section 3, is a modified control algorithm. The algorithm takes into account start-up and shut-down procedures presented in Section 4 and 5 and experimentally verified in Section 6. The paper is concluded in Section 7.

2. Second harmonic compensation

A problem of the pulsating power on the DC side is a common issue of single-phase AC-DC and DC-AC converters. Assuming sinusoidal voltage and current at the AC side:

$$U_t = U_m \cdot sin(\omega t) \tag{1}$$

$$I_t = I_m \cdot sin(\omega t - \phi) \tag{2}$$

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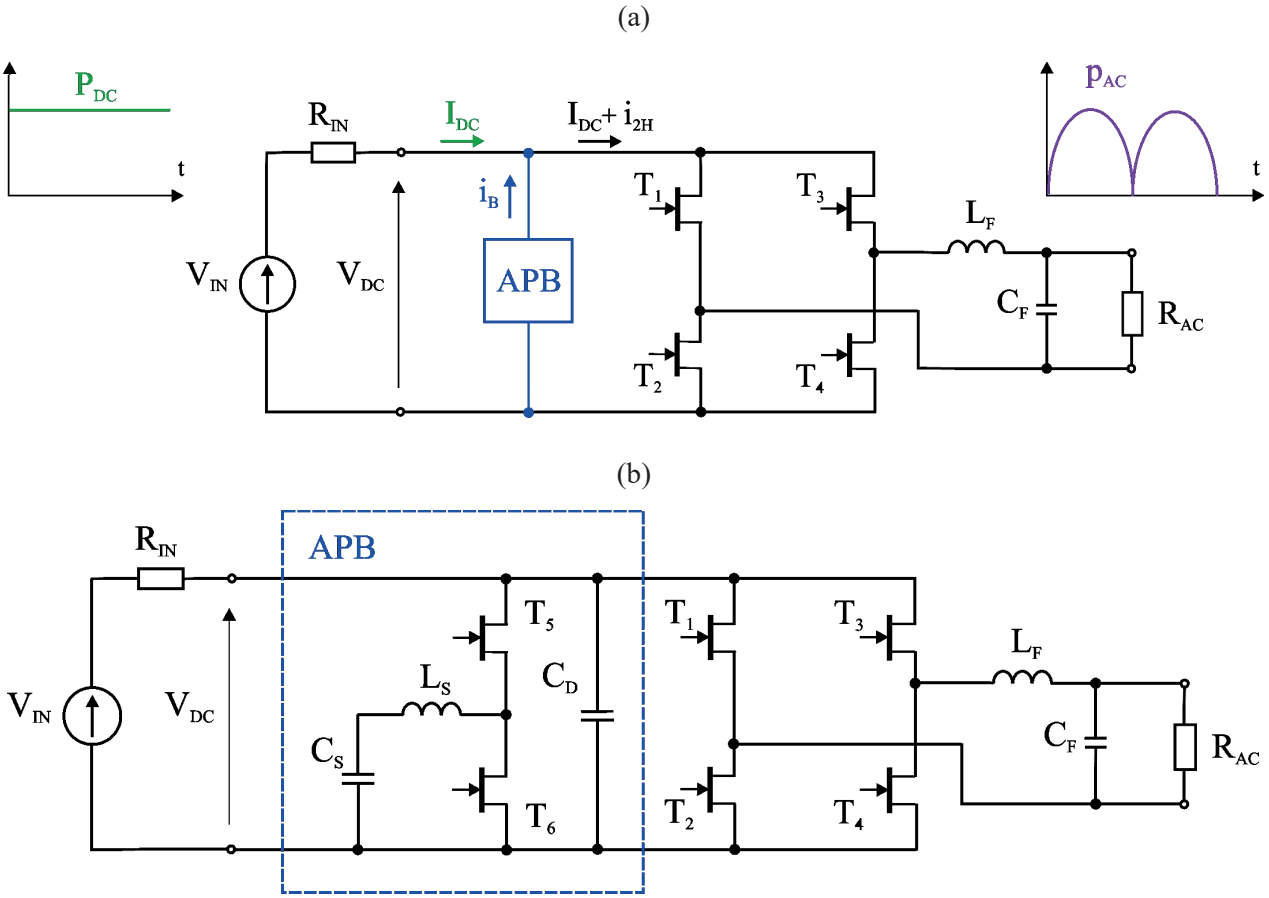


Fig. 1. Basic concept of second harmonic compensation with active power buffer (APB) (a). Scheme of the GaN based H-bridge inverter with active power buffer (b)

an instantaneous power at the DC side can be expressed as:

$$P = u(t) \cdot i(t) = 0.5 \cdot \left(U_m I_m cos(\phi) - \right. \\ \left. - U_m I_m cos(2\omega t - \phi)\right). \tag{3}$$

The equation (3) shows that in addition to a DC component, a second harmonic component of the instantaneous power exists at the same amplitude. As the power at the DC side of the inverter or active rectifier is expected to be constant, power pulsations must be managed due to the second harmonic component. Usually, bulky electrolytic capacitors are applied but this drawback may be solved by active methods. There are different typologies of active power buffer but the main concept is the same – a compensating current in opposite phase to the second harmonic current must be injected into DC circuit of the converter.

An example for the single-phase inverter is presented in Fig. 1a. In order to obtain only DC component I_{DC} at the input, the current of the active buffer I_B should be equal to second harmonic current I_{2H}. In practice, the most common circuit of the buffer uses a capacitive energy storage C_s and chopper circuit to provide suitable compensating current – see Fig. 1b [18]. The operation of this circuit is based on a simple rule – when I_{2H} is positive the APB current is also positive and the storage capacitor is being discharged, otherwise the capacitor is charged. In consequence, the compensation causes a periodic charging and discharging of the Cs – see Fig. 2. Therefore, the buffer requires reasonable capacitance to operate in safe area, $C_s = 120\ \mu$F was applied for 2 kVA inverter in [8].

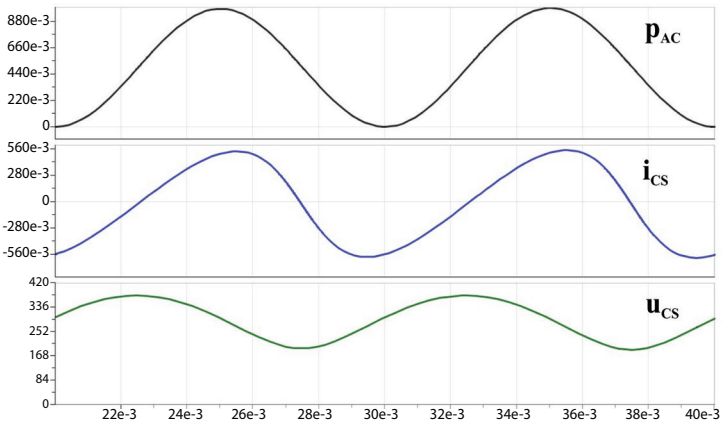


Fig. 2. Simulated waveforms of the inverter with APB (output power pAC, current (iCS) and voltage (uCS) of the storage capacitor Cs)

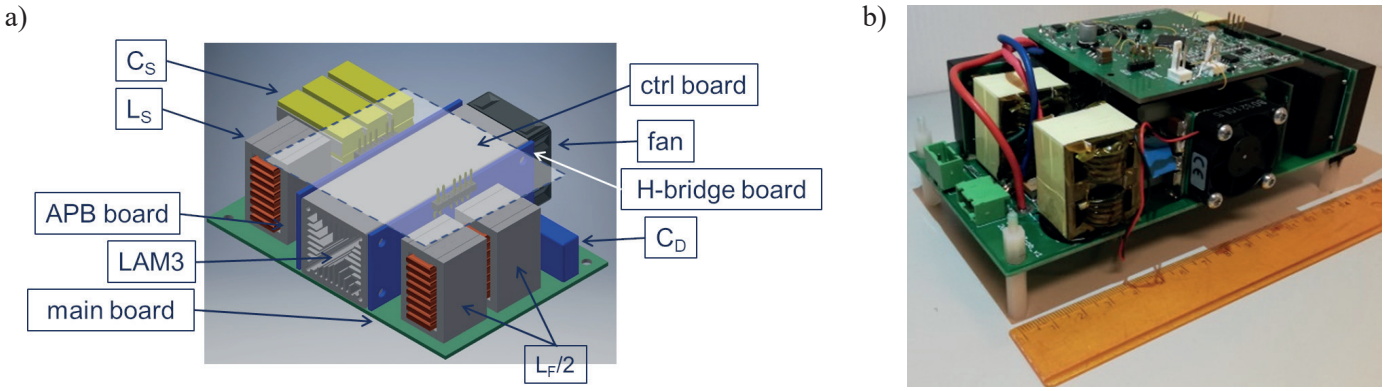


Fig. 3. A visualization (a) and a picture (b) of converter prototype

3. Inverter description

The design presented in this paper was proposed in [7–9, 11, 18] to show an influence of the GaN transistor performance on single-phase inverters. The main circuit presented in Fig. 3a consists of two general active parts: typical H-bridge inverter and additional leg of APB with LC circuit. Each leg of the system (two legs in H-bridge and one leg in APB) uses GaN E-HEMT type GS66508T transistors, which are controlled by Si8274 gate drivers. According to manufacturer recommendations, the positive supply voltage of the gate drivers is set to 7 V, while negative bias equals to –5 V. Each leg of the converter uses a magnetically independent (without coupling) inductor connected between the positive input pole and middle point of the phase leg. The inductors, with an inductance value equal to 40 μH, have been fabricated with use of 3F3 ferrite core material and litz wire constructed with 245 strands, with a diameter of 0.1 mm each. The power losses estimation leads to selection of single heatsink (type LAM3-75-SA) with dimensions of 30×30×75 mm. Due to special design of the fins the heatsinks have relatively low thermal resistance value (Rth), which is at the level of 1.18 K/W (air-forced cooling with air flow at 7.7 m^3/min from fan type: Sepa 30×30×10 mm). The shape of the heatsink allows to mount semiconductors or other heat sources on each of the four side walls. With this in mind visualization and, then, experimental model of DC-AC converter are proposed (Fig. 3b). All semiconductor components have been divided into two groups (H-bridge and APB ones) assigned to own PCB and located on opposite sides of heatsinks to improve thermal dissipation. Finally, the size of the converter is 85×160×50 mm, which results in volume of main circuit approx. 0.68 dm^3 (power density 3 kW/dm^3).

All electrical parameters of semiconductors, inductors and other components are listed in Table 1. This hardware platform was used for further tests of control algorithm.

Table 1
Parameters of the developed 2 kVA converter

Symbol	Quantity	Value
V_1	input voltage range	350–400 VDC
V_2	output voltage	230 VAC/50 Hz
P_n	nominal power	2 kVA
$f_{s(H)}$	switching frequency (H-bridge)	100 kHz
$f_{s(APB)}$	switching frequency range (APB)	100–1000 kHz
$L_{F/2}$	inductance of output inductors	2×40 mH
L_s	inductance of APB inductor	40 mH
$I_{Lm/2}$	inductors maximum current	20 A
C_F	output capacitor	1 mF
C_s	APB capacitor	120 mF/400 V
T_1–T_6	transistors	650 V/50 mΩ (GS66508T)

4. Control algorithm

The fundamental function of the control algorithm presented in Fig. 4a is AC power control, which is usually implemented with resonant controller and pulse width modulator [13, 16]. The active power buffer requires supplementary blocks operating on the base of the suitable voltage and current measurements: the APB controller determines reference value of the current in storage circuit I*, while TCM block is responsible for control of the transistors T_5/T_6 according to triangular current mode principles. Looking at the detailed scheme of the APB controller in Fig. 4b, it can be seen that in addition to standard functions similar to presented in [13, 16], a state detector is proposed and plays crucial role regarding start-up and shut-down processes. As soon as overall control signal ON is activated, the storage voltage V_{CS} is measured and reference current I* is set to I_{CHG} value – this ensures a pre-charging of the capacitor to requested value V_{CS*}. Then, PWM_ON signal starts H-bridge transistors and the reference current I* receives input value from the square wave signal generator until the suitable signal p_{AC_2h} is established on the base of the output current and voltage measurement. The algorithm calculates average value of the output power (P_{AC}) using low pass filter and subtracts it from the pAC value. After several periods p_{AC_2h} contains only AC component and reference current is calculated from:

$$I^* = \frac{P_{AC}}{U_{CS}}. \tag{4}$$

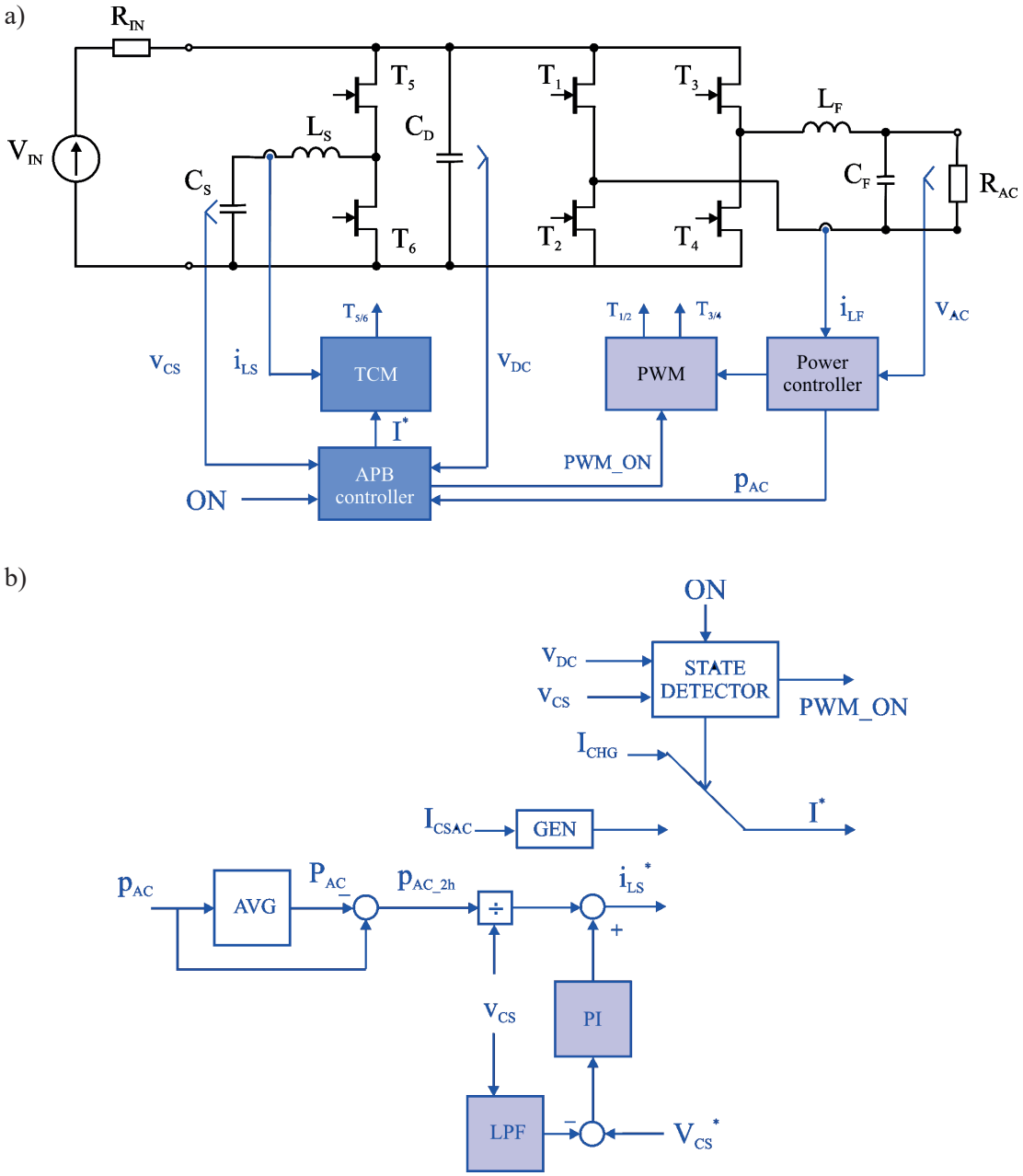


Fig. 4. Block diagram of implemented control algorithm (a) and detailed scheme of the APB controller (b)

This means that APB now can start normal operation mode and compensate second harmonic pulsations. Note that PI controller has to be also applied to ensure that average value of V_{AC} will remain on the requested level. When ON signal becomes low and the H-bridge transistors are stopped by PWM_ON signal, the shut-down procedure is activated. Reference value of the current becomes I_{CHG} but with negative sign, which leads to discharge of the storage capacitor to zero. At this time the inverter is not active and storage capacitor is empty.

In practice experiences show that additional blocks, supporting start-up and controlled shut-down are necessary. Obviously, it is an essential issue to charge energy buffer just before starting compensation since initial energy is required for proper compensation of the pulsating power. This functionality is provided by APB controller block in Fig. 4b.

5. Controller implementation

A hardware prototype has been developed to demonstrate a model of the proposed controller architecture. Taking controlled frequencies into consideration a proposed unit can be divided into two modules: a main bridge controller responsible for forming 50/60 Hz mains waveform for the load circuitry and APB controller module. In the case of the main bridge controller vast majority of measured and processed signals by

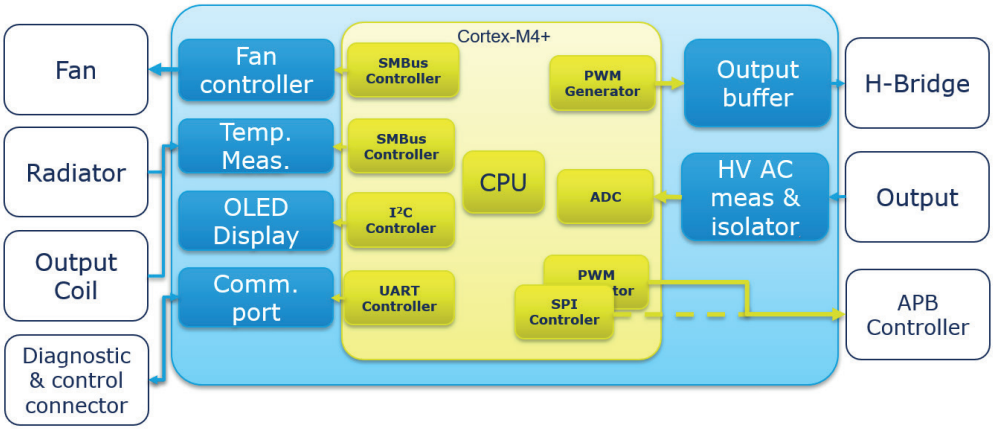


Fig. 5. Block diagram of implemented main bridge controller

this module is relatively slow and can be processed by standard main line microcontroller. This does not apply to output PWM signal driving the H-bridge. On the other hand the effectiveness of 2nd harmonic compensation using TCM modulation is strongly dependent on the triangle waveform frequency [11]. Therefore the APB controller should be able to perform signal processing in real time in relation to the TCM modulating signal. In the presented hardware prototype TCM frequency up to 1 MHz was used. At least 5 MHz bandwidth is required for efficient handling such signals. This requirement is expanded if a digital signal processing is to be used in controller implementation. For this reasons, each of the two controllers has been implemented as a separate module.

5.1. Main bridge controller. A main bridge controller is implemented as a classical digital control system using Cortex-M4+ based microcontroller. A control board is located on top of the stack (Fig. 3a). The main functions of this module are performing measurements of the output voltage and currents, driving output bridge PWM signals and calculating 2nd harmonics for APB controller circuitry. A block diagram is shown in Fig. 5 where all additional functions are listed. The main bridge controller was designed to update every 100 μs, providing PWM duty cycle for main bridge transistors T_1–T_4 and calculating the reference current for APB controller (Fig. 6).

This module contains all necessary measurement circuits providing up to 2 kV isolation from output voltage. Both choke current I_{LF} and output capacitor (V_F) voltage are measured. A measurement circuitry at primary high voltage side is supplied from floating charge pumping power supply. This solution requires an open-loop starting of the controller since for a few first cycles the primary side of measurement circuitry is unpowered (until output voltage reaches value of 40 V_{pp}).

5.2. APB controller implementation. An analog implementation has been settled to provide a sufficient bandwidth and low complexity of the APB controller circuitry. A block diagram of the APB controller is shown in Fig. 6. The main APB control module measures the current at APB circuit on low side measurement resistor, amplifies it by a factor of 2 and compares its value with the reference current Iv from digital module. The resulting signal is used to drive T_5 and T_6 transistors. The reference current I* is set by the main control block based on the calculated 2nd harmonics and by taking into consideration an additional PI control block that ensures sufficiently large energy buffer for compensation circuit to be operational. Additionally, the modulation depth is changed according to DC link voltage to ensure driving of GaN HEMT half-bridges with sufficiently low frequency as shown later. Since base compactor driving

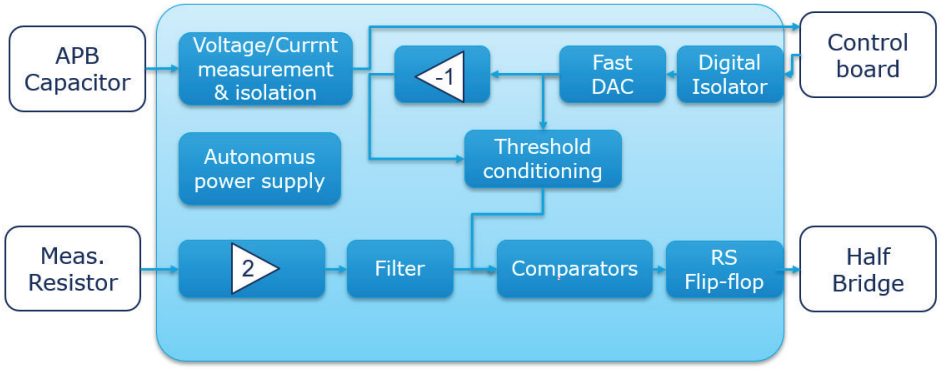


Fig. 6. Block diagram of implemented APB controller

T_5 and T_6 is fully analog and based on RS flip-flop, the APB capacitor cannot be easily kept at given voltage level especially at low reference currents.

6. Results and discussion

The laboratory model of the GaN-based inverter with APB circuit and described above control algorithm were experimentally tested. The system was supplied from the regulated DC-supply via series 10 Ω resistor and loaded with 52 Ω resistive load. In such configuration without active power buffer, a pulsating current from the DC supply is generating swings of the voltage across the reduced DC side-capacitance – as can be seen in Fig. 7. After start of the APB, AC component of the V_{DC} voltage is reduced a few times, however, some fluctuations are still observed due to inaccuracies of the control system (Fig. 8). Another observed phenomenon, which is not studied in this paper but recently discussed in the literature, is a drop of the capacitance with an applied voltage in the Ceralink capacitors [7, 8] – and in consequence a deep discharge of the energy storage. The waveforms presented in Fig. 7 and Fig. 8 confirm a correct operation of the inverter with APB in a steady-state. A mean value of the storage voltage is higher and the mentioned problem can be reduced – the compensating current causes changes by approx. 160 V.

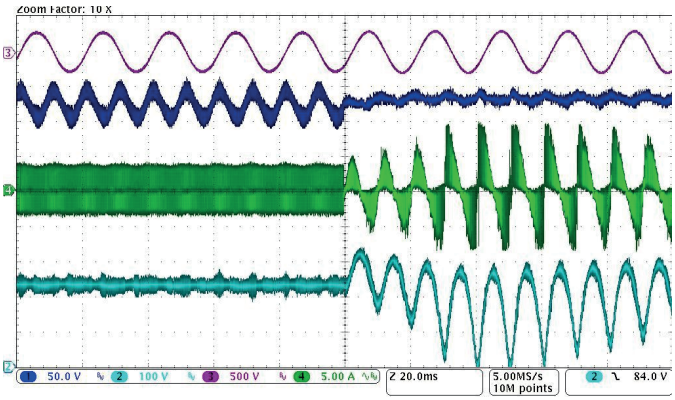


Fig. 7. Waveforms of the output voltage V_{CF}, (500 V/div), the voltage across the DC-side of the inverter V_{DC} (50 V/div), the current of the inductor I_{LS} (5 A/div) and the voltage across the storage capacitor V_{CS} (100 V/div) without and with compensation

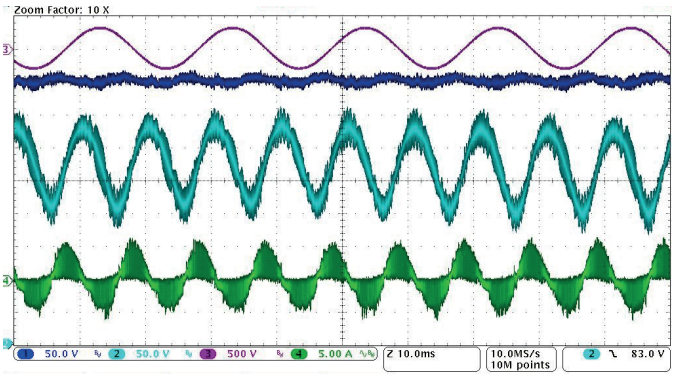


Fig. 8. APB behavior on static V_{cap} drive state. APB current – green, APB capacitor voltage (V_{cap}) – blue, DC link voltage – cyan recorded during steady-state of the APB

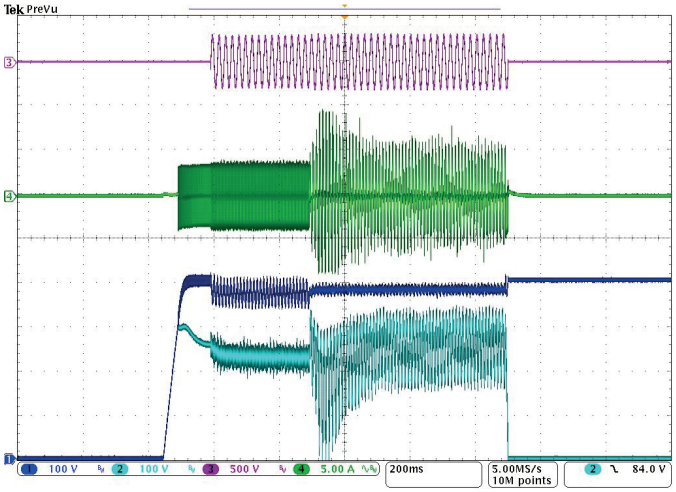


Fig. 9. Waveforms of the output voltage V_{CF}, (500 V/div), the voltage across the DC-side of the inverter V_{DC} (50 V/div), the current of the inductor I_{LS} (5 A/div) and the voltage across the storage capacitor V_{CF} (100 V/div)

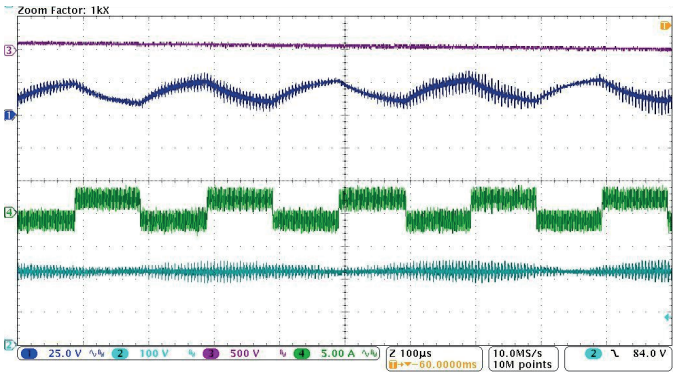
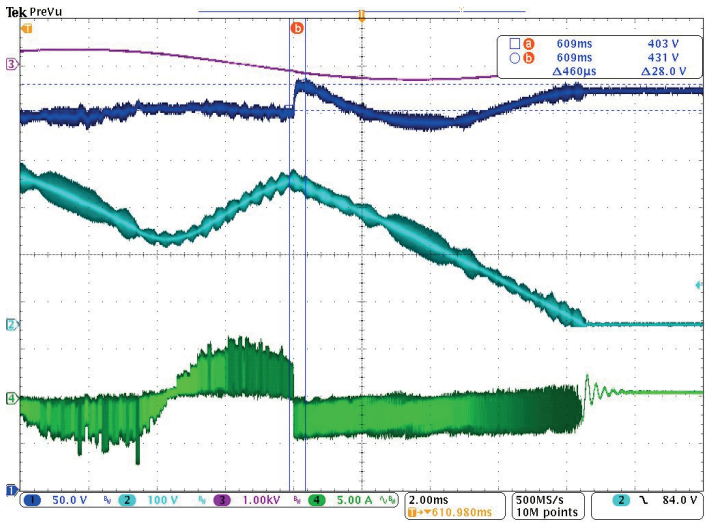


Fig. 10. Waveforms of the output voltage V_{CF}, (500 V/div), the voltage across the DC-side of the inverter V_{DC} (50 V/div), the current of the inductor I_{LS} (5 A/div) and the voltage across the storage capacitor V_{CS} (100 V/div) recorded during steady-state operation of the APB

A scope of this paper is a start-up and shut-down operation of the APB. Therefore, the whole analysis of the system is reduced to approx. 1 s – see Fig. 9. At first, the DC supply is initiated and input DC-side voltage is rising, at the same time, the storage is pre-charged by T_5/T_6 transistors. Then, the inverter starts operation without a compensation as the control system requires some time to correctly determine DC-component of the output power. Without the proper reference value of the pulsating power, the operation of the APB is not recommended and the APB capacitor voltage is kept constant. During this stage, the APB is injecting an AC component as described earlier. According to waveforms in Fig. 10 the peak is set to

(a)



(b)

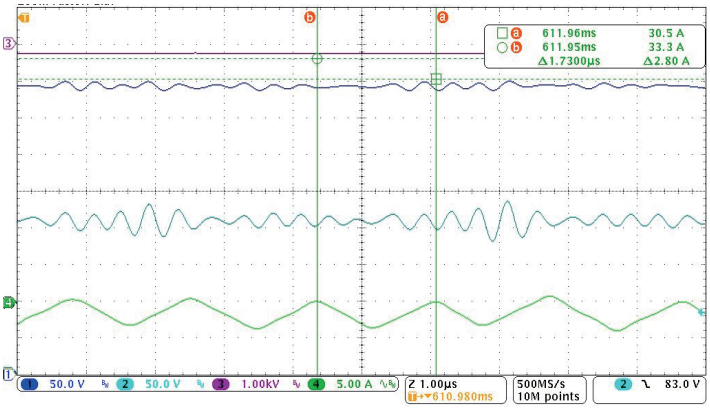


Fig. 11. Waveforms of the output voltage V_{CF}, (500 V/div), the voltage across the DC-side of the inverter V_{DC} (50 V/div), the voltage across the storage capacitor V_{CS} (100 V/div) and the current of the inductor I_{LS} (5 A/div) during shut-down process

4 A in order to keep the switching frequency in the reasonable limit. Then, the APB is activated as was presented in Fig. 7 and, when the inverter is expected to stop operation, the shut-down procedure is initiated – see Fig. 11. The correct shut-down by means of the safe buffer discharge is synchronized with the controller of the output power. Please note that energy from the storage injected to the small DC-capacitor when the inverter is not active will cause an overvoltage and may cause a damage of GaN HEMTs, which are very sensitive to this issue. Thus, the programmed shut down was tested and the measured increase of voltage is around 31 V, which is much below a safety margin of 650 V GaN HEMTs. Another challenge is related to a frequency limit of the T_5/T_6 pair.

For triangular modulation based power buffers an output frequency of transistor gate signal is a product of DC (V_{DC}) and capacitor (V_{CS}) voltages as well as reference current set by the controller (I*) as shown by (5), where t_{boost} and t_{buck} are rising and falling voltage times at C_S given by (6) and (7). As a result the frequency required for proper 2nd harmonic compensation depends on both I* which describes used control algorithm and V_{DC} which is a built-in parameter. For a given I* a maximal frequency is obtained when voltage across C_S

$$f_{APB} = \frac{1}{t_{buck} + t_{boost}} = \frac{V_{Cs}V_{DC} - V_{Cs}^2}{I^* L_s V_{DC}} \tag{5}$$

$$t_{boost} = \frac{I^* L_s}{V_{Cs}} \tag{6}$$

$$t_{buck} = \frac{I^* L_s}{V_{DC} - V_{Cs}} \tag{7}$$

is approximately equal half of V_{DC} which corresponds to $t_{boost} = t_{buck}$:

$$f_{APBmax} \Rightarrow V_{Cs} = \frac{1}{2} V_{DC}. \tag{8}$$

In normal operation, this $2V_{Cs} = V_{DC}$ should correspond to zero output current condition to ensure both equal energy buffer for charging/discharging C_S capability of APB to any load and to ensure that the AC output signal frequency is maximal when output voltage is close to zero. This condition for a power dissipated at switching transistors T_5/T_6 can be kept within operation range even for high switching frequencies. This is accomplished by most of the algorithms presented in the literature. However this approach cannot be used in all operating conditions of the inverter. APB initial charging and discharging of the C_S and an influence of any additional control module used to prevent complete charge/discharge of the C_S (which would make any compensation impossible). Since later case depends on C_S capacitance and it usually results in small I* changes required for maintaining compensation with only slightly decreased parameters. The most significant stress to T_5/T_6 pair is during an initial charging and final discharging as can be seen in Fig. 11a. This problem is particularly essential at high C_S values when both charging current and thus I* are high and charging/discharging time is relatively long. For simple APB control algorithms this problem is quite essential if the input voltage is not constant – for example in battery operation units since maximal switching frequency is dependent on V_{DC} (see (5) and (8)). For the model used in this experiment a maximal frequency (measured during switch-off) vs. DC voltage is shown in Fig. 12.

In order to overcome all inconveniences and to ensure an optimal modulation frequency the charging and discharging current should be modulated based on V_{DC}. In the studied design the control system ensures this by a modulation of discharging current as can be seen in Fig. 12 and recorded waveforms showing switching frequency of 4 A peak storage current below 600 kHz for $V_{DC} = 400$ V, which is reasonably lower than 1 MHz limit.

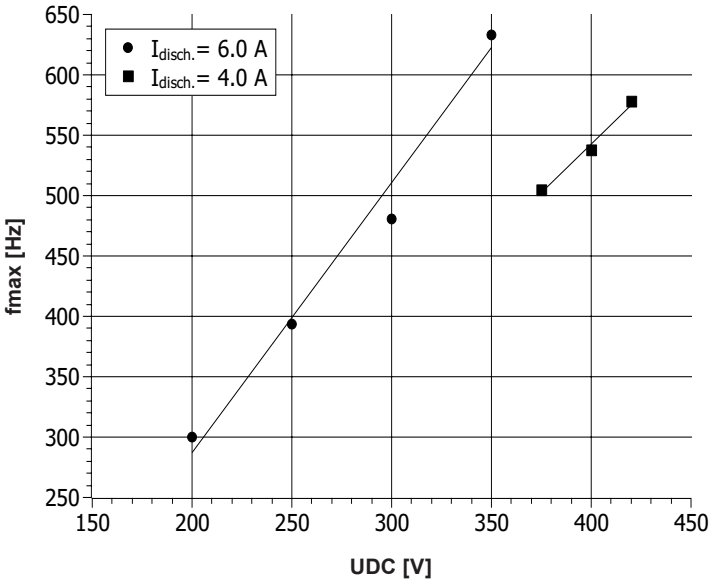


Fig. 12. Maximal frequency during APB circuitry discharging as a function of DC voltage. The bump at the ∼350 V is caused by the change in discharging current

7. Conclusions

The high-frequency active power buffer, which is a subject of this paper, seems to be a good alternative solution to bulky electrolytic capacitors in single phase inverters. In addition to correct and safe operation in a steady-state regime by means of proper control and circuit dimensioning, the APB have to be correctly controlled during start-up and shut down. All proposed modifications of the control algorithm proposed in this paper were experimentally verified. In addition to the compensation of the pulsating power, which is essential function of the discussed circuit, GaN HEMTs are kept in the safe operation range. The voltage upon transistors is always below 450 V, while switching frequency never reaches 1 MHz.

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