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CNTFET Based OTRA and its Application as Inverse Low Pass Filter

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***Abstract*—Operational Transresistance Amplifier (OTRA) has been a topic of great interest recently. OTRA has proved itself to be an appropriate device for the analog applications. As MOS scaling suffers from various problems, carbon nanotube field effect transistor (CNTFET) has came into light as one of the brightest alternative for FET (Field Effect Transistors) based devices. This work has introduced a new CNTFET based OTRA which is capable of realising inverse low pass filter using two OTRAs and few passive elements. CNTFET based OTRA has been designed and simulated at 10nm technology node. The working ability of the designed model has been conformed using HSPICE simulation. It is compared with conventional CMOS based OTRA. The comparative analysis has revealed improvement in various performance parameters. The paper also presents how change in number of carbon nanotube in CNTFETs in OTRA circuit affects the transresistance gain and input impedance. The optimized results are also discussed to improve transresistance gain and input impedance. The paper also dealt with the realisation of inverse low pass filter using proposed CNTFET based OTRA.**

***Keywords*—Carbon Nanotube (CNT), Operational Transresistance Amplifier (OTRA)**

I. Introduction

CURRENT mode (CM) circuits in signal processing have an edge over Voltage mode (VM) circuits. CM technique has better performance in terms of bandwidth, signal linearity, slew rate and power consumption. OTRA as an active element has an advantage that input terminal has current processing capabilities and gives the output as voltage and thus it is able to maintain the compatibility with the present day voltage processing circuits [1].

Operational Transresistance amplifier (OTRA) is an active 3-terminal ABB (analog building block) and its matrix equation is given by:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix}$$

For an OTRA, input and output impedance should be low and transresistance gain, R_m, is to be very high, ideally infinity. Grounded input terminals practically lead the circuits which are not sensitive to the stray capacitance [2]. If negative feedback is applied, the 2- input currents I_+ and I_- will be equal. Complementary MOSFET based Operational Transresistance amplifier realized previously demonstrated very good results at 0.5µm technology node [3]. But scaling down the MOSFET have several issues as short channel effect and process variations and high leakage current thus, circuits realized using highly scaled MOSFET suffers and their performance degrades. Solution of this problem leads to emergence of various efficient devices such as CNTFET, FINFET etc. International technological roadmap for semiconductors (ITRS), recommended CNTFET as a future technology which can replace silicon MOSFET. There are various similarities between CNTFET and MOSFET on the basis of device structure. Thus, CMOS design styles and fabrication infrastructure can be reused. The basic difference between the two lies in the use of carbon Nanotubes (CNT) as the material in the channel in case of CNTFET unlike that of silicon in the MOSFET. CNTs have higher thermal conductivity, higher current densities than most of the metals and semiconductors, higher current mobility [4-7]. This paper conducts the comprehensive study of the CNTFET based OTRA and its comparison with the present technology which is based on CMOS. CNTFET based OTRA has been designed and simulated. All the simulations have been done using HSPICE as per the Stanford 50nm CNTFET SPICE model [8]. The manuscript is structured as follows: Section 2 presents a history of CNTFETs. In Section 3 conventional CMOS based OTRA is presented at 0.18µm technology node and various performance parameters are discussed. Section 4 presents CNT based OTRA and its performance parameters are compared with CMOS based OTRA. This section also deals with the variation of transresistance gain and input impedance by varying the number of CNTs in the specific CNTFETs. Further, optimized results are presented in terms of transresistance gain and input impedance. In Section 5 an inverse low pass filter is realized using two CNTFET based OTRAs and six passive elements. Finally, Section 6 provides the conclusion of the work carried out during this paper.

II. Brief Overview of CNTFET

Carbon Nanotube Field Effect transistor(CNTFET) is an outcome of the evolution of Carbon Nanotubes. It is actually a 4-terminal device that consists of semiconducting carbon nanotube placed between drain and source region, surrounded by the substrate material underneath and its operation is controlled by the voltage applied at the gate. Depending upon the geometry of the CNTFET, they can be classified as planar or coaxial (consisting of wrap-around gate). Planar structure can be further subdivided into top gate CNTFET and back gate CNTFET. On the basis of material composition, CNTFET can be classified as SB-CNTFET and MOS-CNTFET. A Schottky based CNTFET are formed by attaching intrinsic single walled

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CNTs to the metallic source and drain regions. But they are ambipolar in nature. To overcome this, MOS like CNTFET was developed. They are formed by placing CNTs between heavily doped source and drain regions. This resulted in unipolar conduction and larger ON current and low leakage currents. CNTFETs are far better than MOSFETs as channel length of the former can be easily modified up to few nanometers than the later, ballistic conduction is possible in CNTFETs but not in MOSFETs, gate capacitance is higher in CNTFET which enables faster switching. As the CNTFET gate can be better controlled, consequently transconductance is higher in CNTFET. Threshold voltage is lower in CNTFET which causes low power dissipation. Properties of carbon nanotubes can be easily modified to form metallic, semiconducting or insulating material by varying their diameter, length and Chirality vector [n,m]. If n-m is equal to 3k where k is an integer, the nanotube will behave as an conductor, otherwise it is a semiconductor. Energy gap of semiconducting CNTs can be easily modified by changing its diameter. The relation between threshold voltage V_{th}, and band gap E_g is given by equation (i)

$$V_{th} = \frac{E_g}{2e} = \frac{a_0 E_\pi}{eD_{CNT}} \approx \frac{0.43}{D_{CNT}} \quad (1)$$

The diameter of the CNT can be varied by varying the chirality vector [n,m] in accordance to the equation (ii).

$$D_{CNT} = \frac{\sqrt{3}a_0 \times \sqrt{n^2+m^2+nm}}{\pi} \approx 0.0783 \times \sqrt{n^2+m^2+nm} \quad (2)$$

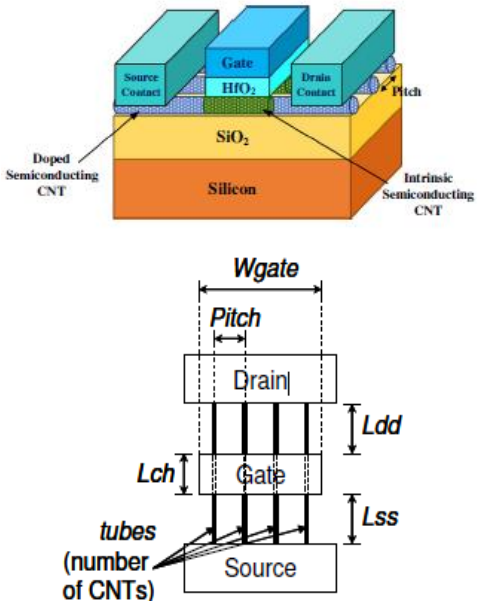

Fig 1. Scheme of CNTET (a) Top view, (b) 3D View

III. CMOS BASED OTRA

The realization of OTRA using CMOS was given by Salama and Soliman [3]. Circuit proposed by them is shown in Fig 2. Downscaling of MOSFET, leads to degradation of the performance of CMOS based circuits. So, to analyze the effects of downscaling the simulations were performed on 180 nm technology node using HSPICE. The model parameters of NMOS and PMOS are working at 0.18µm technology node.

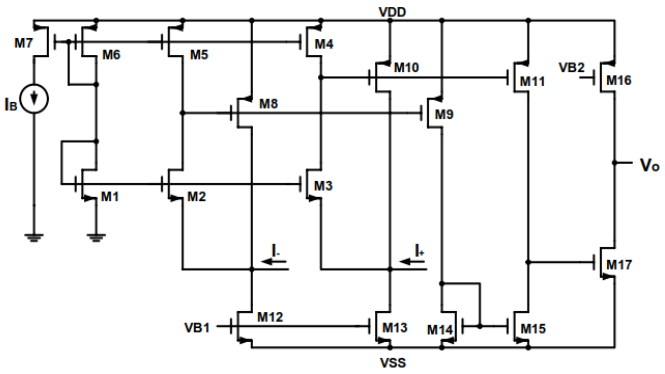

Fig 2. OTRA realization proposed in Salama and Soliman.[3]

The biasing current I_B is 25µA. The biasing voltages V_{B1} = -0.5 V and V_{B2} = 0.1 V. The aspect ratios of the transistors used in [3] is given in Table I. Simulation results are shown in Figs. 3, 4 and 5.

TABLE I
TRANSISTOR ASPECT RATIO IN OTRA CIRCUIT [3]

Transistor	W/L ((µm)
M1-M3	36/.9
M4-M11	18/.9
M12,M13	10.8/.9
M14,M15	18/.9
M16	3.6/.9
M17	18/.18

The V_{out} of OTRA, when the inverting input is examined from -50 mA to 50 mA for the various values of the non-inverting input is shown in Fig. 3. For the proposed CMOS based OTRA, R_{in} is 22.3Ω (Fig.4). Open loop DC transresistance gain is 64.7 dBΩ (= 1.7 KΩ) (Fig.5). Gain x bandwidth is 59.4 GHzΩ (Fig.5). Power dissipation of given circuit is 5.07 mW. Frequency response for open loop transresistance gain for the CMOS based OTRA is shown in Fig.5.

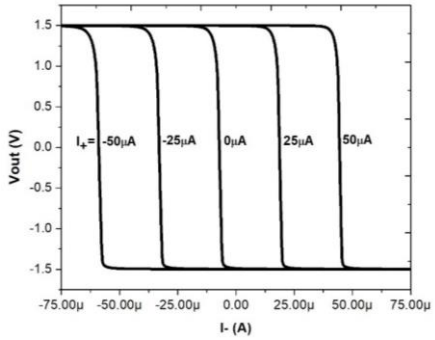

Fig. 3. V_{out} of the CMOS circuit

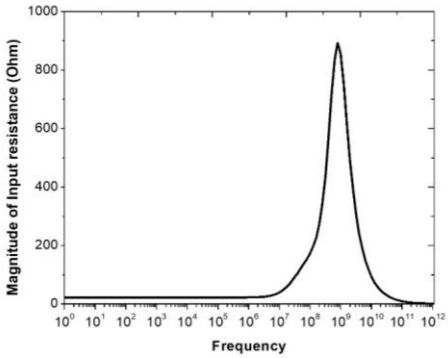

Fig.4. Input Resistance at positive input terminal for the CMOS circuit

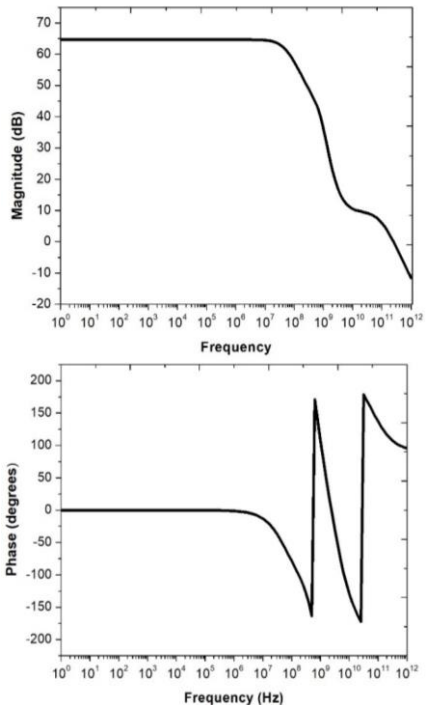

Fig 5. Frequency response of the open loop transresistance gain for the CMOS circuit

IV. Proposed CNTFET based OTRA

Symbol of CNTFET based Operational Transresistance Amplifier is shown in Fig 6.

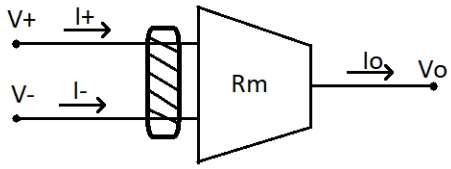

Fig.6. Block diagram of the CNTFET based OTRA

This paper presents CNTFET based OTRA which has been designed and compared with CMOS based OTRA. Fig.6 shows the block diagram of proposed CNTFET based OTRA. PCNTFET and NCNTFET both have the same mobility. The proposed circuit (Fig.7) uses both PCNTFET and NCNTFET which has similar structure to the Salama and Soliman proposed model.

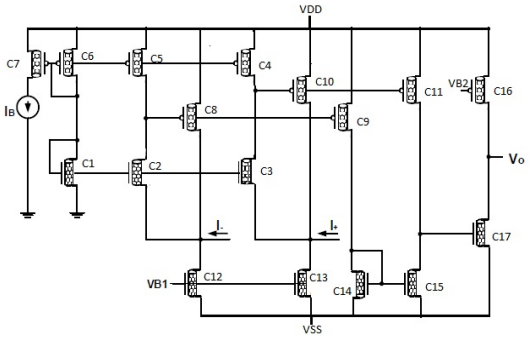

Fig.7. Proposed CNTFET based OTRA

TABLE II
PARAMETERS OF CNTFET

Device parameter	Values
Work Function (CNT)	4.5eV
Dielectric constant	16
Gate oxide	HFO_2
Pitch	20nm
Power supply	±2V
Mean Free path :Doped CNT	12.5nm
Physical Channel Length (L_{ch})	32nm
Mean Free path :Intrinsic CNT	200nm
Chirality of tube(m,n)	19,0

TABLE III
NO. OF TUBES AND LENGTH OF CHANNEL OF CNTFETS IN CIRCUIT SHOWN IN FIG.7

CNT-Transistor	No. of tubes	L(nm)
C1-C3	11	50
C4-C11	6	50
C12,C13	4	50
C14,C15	6	50
C16	2	50
C17	6	10

A. *Simulations results and analysis*

In this section, CNTFET based OTRA introduced previously has been simulated and compared with its CMOS counterpart. Synopsys HSPICE simulator has been used to conduct the simulations as per the Stanford SPICE Model [8] for CNTFET with feature size of 10-nm which includes parasitics as well as non-idealities. The concise description of CNTFET parameters is reported in Table II and the corresponding values of these parameters have been specified. Table III shows number of tubes and channel length of the CNTFET model used to simulate the OTRA.

Bias current I_B = 25µA. Bias voltages, V_{B1} = -0.5 V and V_{B2} = 0.1 V.The acquired results are as under. Range of differential input current is -50µA to 50µA (Fig.8). Input resistance is 1.72KΩ (Fig.9). The DC open loop transresistance gain is 95.6 dBΩ (= 60 KΩ) (Fig.10). Gain x Bandwidth is 5.34 THz.Ω (Fig.10). Power dissipation of the circuit is 0.7 mW.

From Fig. 5 and Fig. 7 we have conculded that the transresistance gain has increased from 64.7dBΩ to 95.6dBΩ The gain bandwidth product has increased tremendously from 59.4GHzΩ to 5.34THzΩ. The power dissipation also decreases from 5.07mW to .7mW. But the input resistance is not as low as it was expected. The comparison is presented in Table IV.

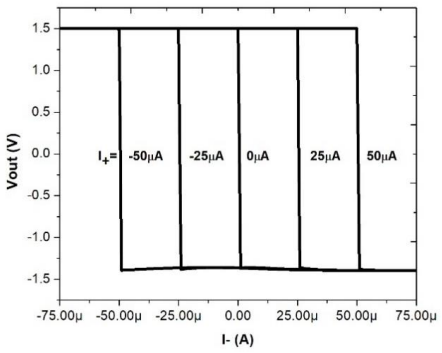

Fig.8. The output voltage of the circuit

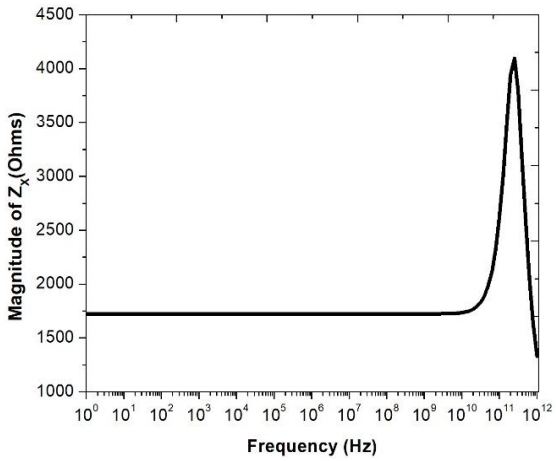

Fig. 9. CNTFET based OTRA input impedance

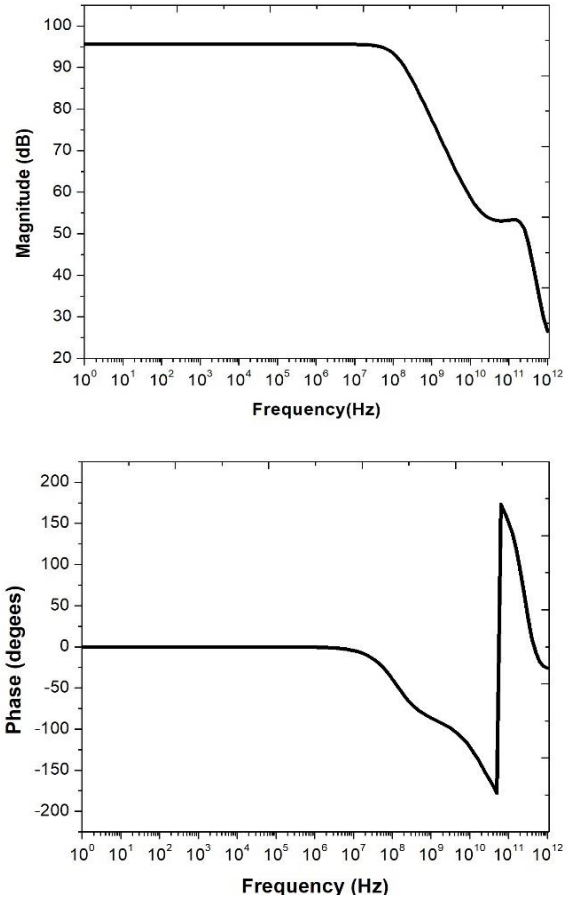

Fig. 10. Frequency response of the open loop transresistance gain

TABLE IV
COMPARISON OF SALAMA & SOLIMAN OTRA MODEL WITH THE PROPOSED CNTFET BASED OTRA MODEL

Parameter	Salama and Soliman OTRA	Proposed CNTFET based OTRA
Input current dynamic range(μA)	-50 to 50	-50 to 50
DC open loop transresistance gain(dBΩ)	64.7	95.6
Gain x bandwidth in (GhzΩ)	59.4	5340
R_{in} in ohms	22.3	1720
Power dissipation(mW)	5.07	0.7

Some exemplary observations were made during the study of the proposed CNTFET based OTRA model. These are given below.

1. The last stage of OTRA has a common source amplifier (C_{17}), it was observed that the gain of the proposed CNTFET based OTRA can be increased by increasing the conductance of C_{17}. By increasing no. of CNTs in CNTFET, current driving capability of CNTFET increases and hence gain of common source amplifier increases which in turn increases transresistance gain of the OTRA, this is clearly depicted by Fig.11. The Open loop transresistance gain increases linearly from 60.3KΩ to 346.8 KΩ with linear variation of CNTs from 6 to 35.

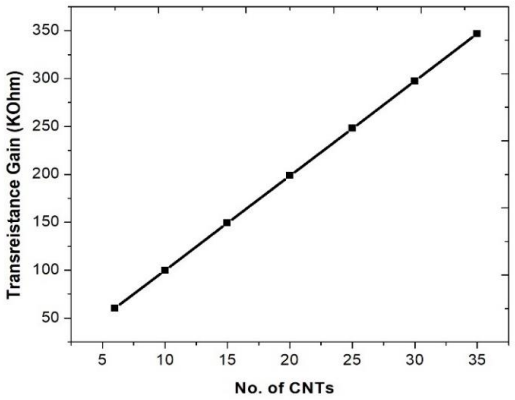

Fig.11. Variation of transresistance gain of OTRA with no. of CNTs.

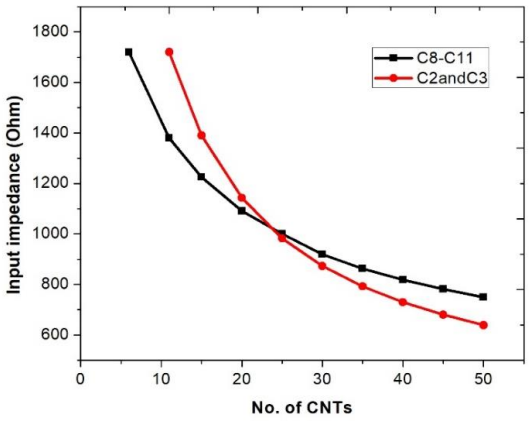

Fig. 12.Variation of input impedance with no. of CNTs

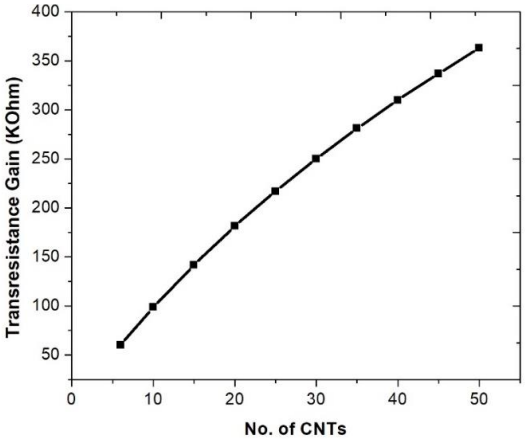

Fig.13. Variation of gain with no. of CNTs in C8-C11

2. In the input stage, C_2 and C_3 affect the input impedance of OTRA. This effect is independent of transresistance gain and other parameters. When the number of tubes are incremented in C_2 and C_3, input resistance can decrease (should approach to zero ideally), this can be seen in Fig.12. The current mirrors (C_8, C9) and (C_{10}, C11) are used in current differencing operation and thus influences both input impedance and transresistance gain. With increase in CNTs the decrease in input impedance here is more gradual than it was with input stage (Fig.12). The Fig.13 reports the change of transresistance gain with increase in number of CNTs of C8-C11.
3. C_{12} and C_{13} affect both input impedance and transresistance gain. So, increasing no. of CNTs in these CNTFETs results in a dramatic increase in transresistance gain and decrease in the input impedance simultaneously. But an attempt to increase number of tubes beyond 9 deviates the curves and impedance starts increasing and gain decreasing. The Fig.14 and Fig.15 shows these results. Here, the caution for the readers is that increasing no. of CNTs in C_{12} and C_{13} can upset the DC characteristics of OTRA.

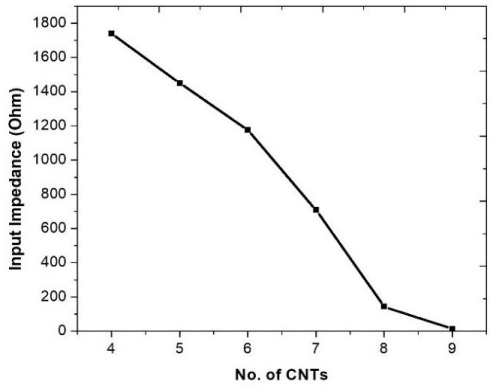

Fig.14. Variation of input impedance with no. of CNTs

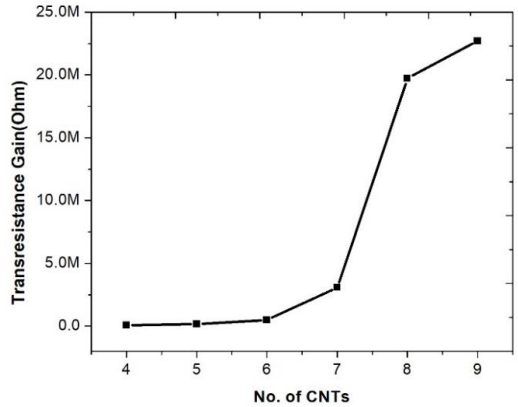

Fig.15. Variation of Transresistance gain with no. of CNTs

B. Optimized Results

The DC characteristics of OTRA are not affected and differential range of input current is varying from -50µA to 50µA. The DC open loop transresistance gain is equal to 154.23dBΩ (51.5MΩ). The product of gain and bandwidth is 1.264Thz.Ω. The circuit power dissipation is equal to 1.36mW. The results are optimized in terms of transresistance gain and input impedance but there is a trade off that Gain Bandwidth product decreases and Power Dissipation increases but that is in the acceptable limits. The Table V shows the number of CNTs and channel length of CNTFETs used in the simulation of optimized results and the optimized results are compared in the Table VI.

TABLE V
NO. OF TUBES AND LENGTH OF CHANNEL OF CNTFETS USED IN THE OPTIMISED CIRCUIT

CNT Transistor	No. of tubes	Length (nm)
C1	11	50
C2,C3	100	50
C4-C7	6	50
C8-C11	100	50
C12-C15	6	50
C16	2	50
C17	15	10

TABLE VI
COMPARISON OF THE PREVIOUS RESULT OF CNTFET BASED OTRA WITH THE OPTIMIZED RESULTS

Parameters	Previous Results	Optimized Results
Input Current dynamic range(µA)	-50µA to 50µA	-50µA to 50µA
DC Open loop transresistance gain(dBΩ)	95.6	154.23
Gain Bandwidth product(THz.Ω)	5.34	1.264
Input Resistance(Ω)	1720	109
Power Dissipation(mW)	.7	1.36

V. APPLICATION OF CNTFET BASED OTRA AS AN INVERSE LOW PASS FILTER

Inverse filters are important building block of any communication system and control systems. They are commonly used in communication, audio and acoustic system, speech and image processing and instrumentation. An inverse filter is used to reverse the distortion incurred during the signal processing and transmission of signals. It is used at the receiver's side and should possess an inverse transfer function to that of the original signal so that when a distorted signal is fed at the input, an undistorted signal is produced at the output.

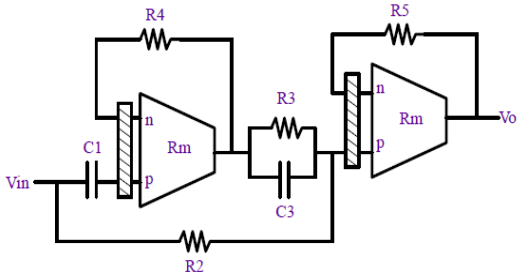

Fig.16. Inverse low pass filter using CNTFET based OTRA

The given model of OTRA based inverse filter was first proposed by Singh, Gupta and Senani in [9], that involved the usage of two OTRA's and five to six passive elements and was realized using 0.18µm CMOS technology. Here we proposed the same structure using CNTFET based OTRA using 10nm CNTFET technology has been proposed which is shown in Fig.16 and further workability of an inverse low pass filter are justified using HSPICE simulations.

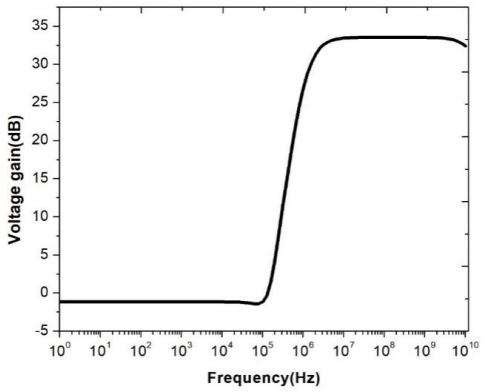

Fig. 17 Frequency response of proposed filter

The given circuit could be used to realize all the basic inverse filters by varying the elements of the model. The parameters that are adjusted to form inverse low pass filter are:

$$Y_1 = sC_1 \ , \ Y_2 = \frac{1}{R_2}, \ Y_3 = sC_3 + \frac{1}{R_3} \ , Y_4 = \frac{1}{R_4}, \ Y_5 = \frac{1}{R_5}$$

The transfer function for inverse low pass filter is given by:

$$\frac{V_0}{V_{in}} = \frac{1}{\frac{\frac{R_2}{R_5}\left(\frac{1}{C_1C_3R_2R_4}\right)}{s^2+s\left(\frac{1}{C_3R_3}\right)+\frac{1}{C_1C_3R_2R_4}}} \quad (3)$$

The inverse low pass filter frequency response is given in Fig.17.

VI. Conclusion

This paper presents CNTFET based Operational transresistance amplifier. OTRA has several advantages over conventional operational amplifiers. A fair comparison has been made between conventional CMOS based OTRA and CNTFET based OTRA. A few observations have also been presented for changing the number of CNTs of specific CNTFET in the circuit affects the performance of the OTRA. Finally, using the observations optimised results has also been reported. The results are far better than the conventional CMOS based OTRA. An inverse low pass filter using CNTFET based OTRA is also introduced.

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