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The flying-capacitor SEPIC converter with the balancing circuit

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Abstract: The paper presents investigation results of the natural balancing phenomena in the flying-capacitor SEPIC converters. The SEPIC converters topologies can be reconfigured to the flying-capacitor topology. Owing to this modification the advantageous increase of frequency of the current in the chokes and the decrease of semiconductors voltages can be achieved which is shown in this paper. Similarly to other multilevel flying capacitor topologies the adequate voltage sharing of the flying capacitors is an important issue for safe operation of the converter. The paper focuses on the analysis of the flying capacitor voltages balancing in the converter by natural currents as well as by the application of the additional RLC balancing booster. The paper proves that the natural balancing can be achieved by the specific application of the balancing circuit in the flying-capacitor SEPIC topology and proves the specific differences in the balancing process by natural currents of converter and with the usage of the balancing circuit. An operation of the converter with the balancing circuit and the natural balancing ability is studied here.

Key words: SEPIC converter, natural balancing, flying-capacitor

1. Introduction

The switch-mode DC-DC converters are commonly used in power electronic systems [1-15]. At the same time, multilevel converters remain the subject of interest of many researches [1-7, 16-27]. There are plenty of new ideas of novel topologies as well as modifications of typical converters. In [1-7] one of the ideas of modification of the switch-mode converters into multilevel topologies is presented. The converters in the flying-capacitor topologies can operate with decreased voltage stress on semiconductors and increased frequency of AC components of currents and voltages.

The SEPIC converters is one of the most popular boost-buck converter in the battery fed applications, such as LED lighting systems [13] but also in other fields [14, 15] where the continuous input current with the boost-buck operation is advantageous. The SEPIC converter in the flying-capacitor topology is demonstrated in [2] as well as in [3-5] in modified three-level

topologies. In the flying-capacitor topologies a proper balancing of voltages on flying capacitors is one of the crucial issues for proper operation of the converter. For the switch mode DC-DC converters the problem is addressed in [1] where the method of natural balancing of the flying-capacitor boost and buck-boost converter is presented, but the SEPIC topology is not analyzed there. The flying-capacitor SEPIC converter is the more complex topology than e.g. a boost converter by the application of additional LC components. This paper demonstrates that the flying-capacitor SEPIC converter can also achieve the natural balancing capability. It will be realized by the specific application of the balancing RLC booster. The paper addresses the detailed analysis and proof of the natural balancing process that occurs with the use of the additional RLC booster as well as the natural internal currents of the multilevel SEPIC converter. The natural voltage balance of capacitors applied in multilevel topologies is an issue discovered for flying-capacitor-type converters [22-23] but also H-Bridge converters [24] and NPC converters [25-27].

The paper presents an analysis of the operation of the flying-capacitor SEPIC converter focusing on the following aspects:

– operation of the converter and voltages on switches,
– conditions necessary for triggering and achieving the natural balancing process,
– flying capacitors recharging by the internal current components,
– operation of the converter with the balancing booster,
– current and voltage components on the additional LC components.

Furthermore, the presented analysis discovers more deeply than in [1] the relationship between unbalancing and selective stabilization of the converter by the internal and balancing current. The analytical discussion is verified by Matlab/Simulink simulation results.

2. The flying-capacitor SEPIC converter

Fig. 1 presents the topology of the flying-capacitor DC-DC converter. In the analyzed case the converter is composed as the 3-cell topology but in a general case another number of cells can be used.

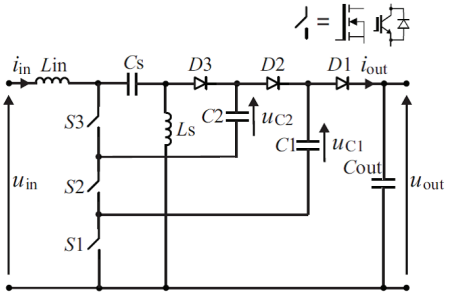

Fig. 1. The DC-DC SEPIC converter with two flying-capacitor cells

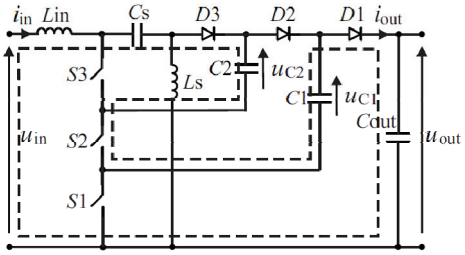

Fig. 2. An example of current flow in the DC-DC SEPIC converter with two flying-capacitor cells

The analyzed converter utilizes two flying capacitors. The transistor and diode branches are composed with 3 components respectively. The current flows via switches and flying capacitors which affects voltage on switches and choke as well as the choke frequency. Fig. 2 presents an example of the current flow in the converter. To achieve the proper modulation, similarly as in [1], the suitable PWM method is implemented, where the control signals *Sn* for a corresponding transistor has the same duty cycle and one third of a period phase shift. PWM can be achieved as carrier-based phase shifted PWM.

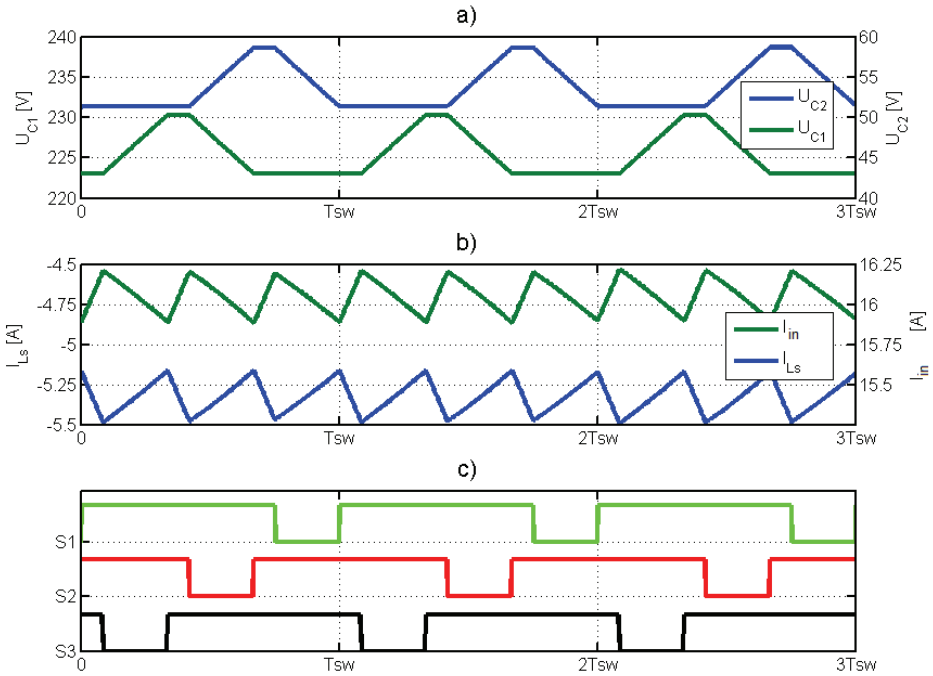

Fig. 3. The steady state CCM waveforms in the DC-DC SEPIC converter with two flying-capacitor cells: the flying capacitors voltages (u_{C1}, u_{C2}), inductors currents (i_{Lin}, i_{Ls}), power switches control signals (*Sn*); U_{out} = 400 V, P_{out} = 2 kW, D = 0.75 and other of parameters according to Table 1

The single switch is controlled by the signal *Sn* with the switching frequency f_{sw}. In such conditions the AC component of the input inductor has frequency of $3f_{sw}$. This is the same

feature as in the converters presented in [1] and can be seen in Fig. 3 that presents the steady-state operation of the 3-cell SEPIC converter. The SEPIC converter utilizes an auxiliary choke and capacitor in the topology (L_s and C_s Fig. 1).

Under steady state conditions the voltage ratio of the described converter is the same as for typical SEPIC converter and is given by:

$$k = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{D}{1-D}, \tag{1}$$

where: D is a duty cycle of Sn switching signals

The application of the flying-capacitors in the DC-DC SEPIC converter makes it possible to achieve a decreased voltage of semiconductor switches. The maximum voltages across power switches and diodes are given by:

$$U_{D1\_\max} = U_{SP1\_\max} = U_{C\text{out}} - U_{C1}, \tag{2}$$

$$U_{D2\_\max} = U_{SP2\_\max} = U_{C1} - U_{C2}, \tag{3}$$

$$U_{D3\_\max} = U_{SP3\_\max} = U_{CS} + U_{C2}. \tag{4}$$

If the voltages across the switches and the diodes given by (2)(4) are assumed to be equal in balanced state, the following relations could be written (omitting ripple):

$$U_{C\text{out}} - U_{C1bal} = U_{C1bal} - U_{C2bal} = U_{CS} + U_{C2bal} = U_{SPD}, \tag{5}$$

where:

U_{SPD} is the voltage across the switches and diodes used in further analysis

U_{C1bal}, U_{C2bal} are the voltages across the capacitors C_1, C_2 in balance state

For further analysis it can be assumed that the capacitance of C_s, C_1 and C_2 is big enough for treating voltage across them as constant. During the steady state operation of the converter, the average values of u_{cs} and u_{in} are the same. Due to the very low ripple of u_{cs} it could be assumed that:

$$u_{CS} = u_{\text{in}} = \text{const}. \tag{6}$$

It could be derived from (5) and (6) that voltages across capacitors C_1 and C_2 in a balanced state, are given by:

$$U_{C1} = \frac{2}{3}U_{\text{out}} - \frac{1}{3}U_{\text{in}}, \tag{7}$$

$$U_{C2} = \frac{1}{3}U_{\text{out}} - \frac{2}{3}U_{\text{in}}. \tag{8}$$

Using formulas (2)(8) the maximum voltage across power switches and diodes under a balanced state is derived:

$$U_{SPD} = \frac{1}{3}(U_{\text{out}} + U_{\text{in}}). \tag{9}$$

The formula (9) can be combined with the expression describing output voltage (1):

$$U_{SPD} = \frac{1}{3}U_{\text{in}}\frac{1}{1-D}. \tag{10}$$

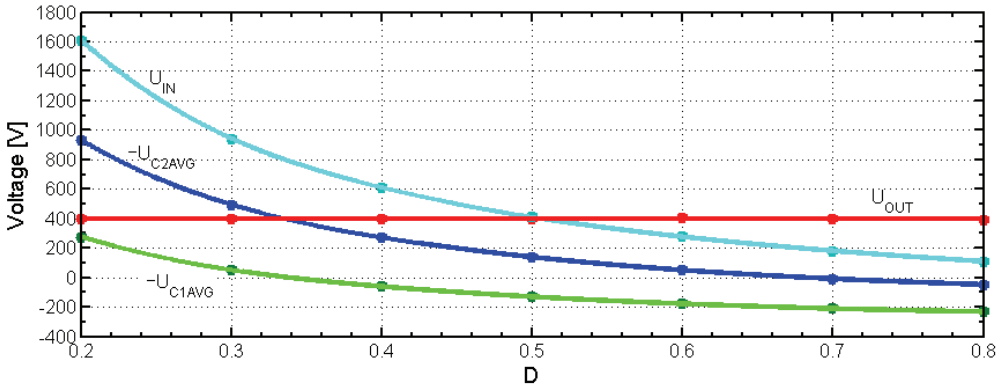

Fig. 4. The average voltage measurements of the flying-capacitors DC-DC converter vs. duty cycle (D) for U_{out} = const = 400 V, P_{out} = 2 kW (R_d = 78.8 Ω). CCM operation. Matlab/Simulink simulation results

Equations (6) to (10) are true only under the steady state of the converter with appropriate flying capacitors voltage sharing but shows the beneficial voltage decrease on semiconductor switches in relation to the basic SEPIC topology. The maximum voltages across the switches are determined by the voltages on the flying-capacitors in the converter. These voltages as well as the voltage on the series capacitor C_s vary with the input and output voltages. Fig. 4 presents average voltages on the flying-capacitor SEPIC versus the duty cycle under the balanced state.

3. Balancing of the flying-capacitor voltages of the SEPIC converter and application of the balancing circuit

Under the unbalanced state in the flying-capacitor converter the voltages of semiconductor switches rise and the risk of failure increases. In order to maintain the balanced state in the SEPIC converter the RLC balancing booster [1] can be used. Fig. 5 presents the balancing circuit implementation in the flying-capacitor SEPIC converter. The balancing circuit can be connected to the point M as well as N. Both nodes (N and M) are connected together by capacitor C_s which for balancing current frequency has negligibly low reactance.

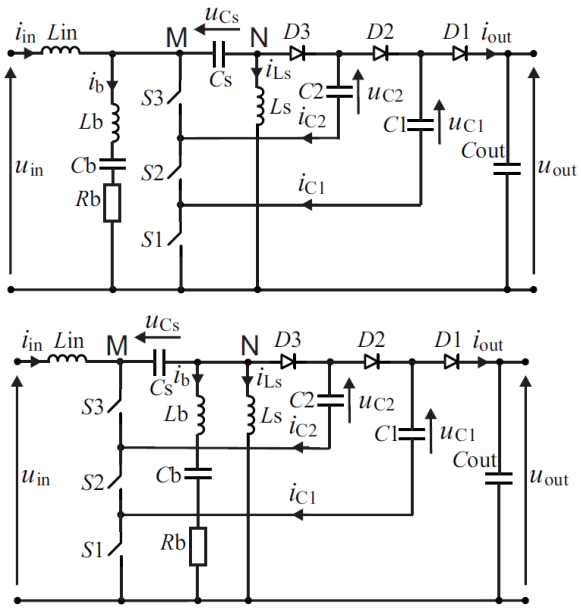

Fig. 5. The balancing circuit connection in the flying-capacitor SEPIC converter

Thus, there is no important difference in the balancing process between the case of connection balancing branch to node *M* or *N*. However, some practical reasons may be important, because the voltage across the balancing branch connected to the point *N* has no DC component. Thus, the peak voltage across the balancing branch connected to the node *N* is definitely lower which affects the size of balancing capacitor C_b. In the Fig. 6 the voltages across the balancing branch connected to the point *N* and *M* are presented in the time and frequency domain. Results are obtained for the balanced as well as the heavily unbalanced converter during the steady state of the operation. The balancing current will arise in this circuit under the unbalanced state only, to prevent purposeless power losses under the balanced state of the converter. Thus, the selective resonant circuit is utilized in the balancing branch, which has the resonant frequency adjusted for the u_M (or u_N) voltage frequency under the unbalanced state f_{sw}. The current of the flying capacitors is determined by control which can be described by the formulas:

$$i_{C1} = (i_{\text{in}} - i_b - i_{Ls})(S1(t) - S2(t)), \tag{11}$$

$$i_{C2} = (i_{\text{in}} - i_b - i_{Ls})(S2(t) - S3(t)), \tag{12}$$

where:

$Sn(t) = 1$ if control signal for *Sn* transistor is high, whilst,

$Sn(t) = 0$ if control signal for *Sn* transistor is low.

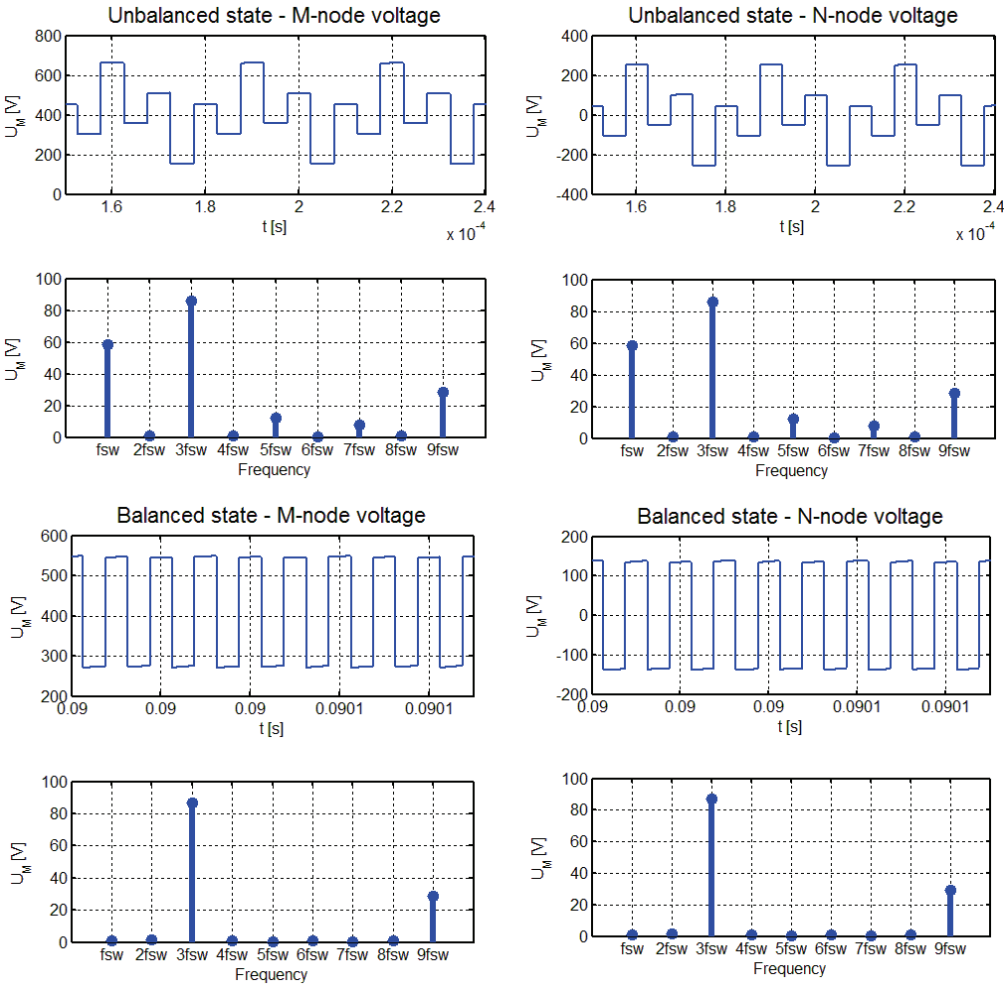

Fig. 6. Voltage in node *M* and *N* under the balanced and unbalanced state presented in time and frequency domain. $U_{out} = 400$ V, $P_{out} = 2$ kW ($R_d = 78.8\ \Omega$), $D = 0.5$. Matlab/Simulink simulation results

The balancing process can occur only when the cycle mean value of currents i_{C1} or i_{C2} or both can be nonzero. Due to the orthogonality of harmonics, this condition may be satisfied only when the current (i_{in}-i_b-i_{Ls}) contains the harmonic that corresponds to the harmonic of at least one of the functions:

$$s_1(t) = (S1(t) - S2(t)), \tag{13}$$

$$s_2(t) = (S2(t) - S3(t)). \tag{14}$$

Functions (13) and (14) have harmonic with f_{sw} frequency however the harmonic with 3 f_{sw} does not exists, due to $2\pi/3$ phase shift between each *Sn* signal. Thus, only the f_{sw} harmonic of current (i_{in}-i_b-i_{Ls}) can cause the balancing of the flying-capacitor voltages. Higher

than $3f_{SW}$ harmonics of the current (i_{in}- i_b- i_{Ls}) and functions (13)(14) have negligible influence on the balancing process due to their low amplitudes. Approximation in the first harmonic domain of functions (13) and (14) is given by:

$$s_{1(f_{SW})}(t) = C\left[\sin(\omega_{sw}t) - \sin\left(\omega_{sw}t - \frac{2\pi}{3}\right)\right] = \sqrt{3}C\sin\left(\omega_{sw}t + \frac{\pi}{6}\right), \tag{15}$$

$$s_{2(f_{SW})}(t) = C\left[\sin\left(\omega_{sw}t - \frac{2\pi}{3}\right) - \sin\left(\omega_{sw}t + \frac{2\pi}{3}\right)\right] = \sqrt{3}C\sin\left(\omega_{sw}t - \frac{\pi}{2}\right), \tag{16}$$

where: C is a constant which depends on duty ratio of Sn, $\omega_{sw} = 2\pi f_{sw}$

In the f_{SW} frequency domain the formulas (11) and (12) have the following form:

$$i_{C1(f_{SW})} = \sqrt{3}C(i_{in} - i_b - i_{LS})\sin\left(\omega_{sw}t + \frac{\pi}{6}\right), \tag{17}$$

$$i_{C2(f_{SW})} = \sqrt{3}C(i_{in} - i_b - i_{LS})\sin\left(\omega_{sw}t - \frac{\pi}{2}\right). \tag{18}$$

Currents i_{in} and i_{Ls} exist naturally in the converter, but they are known to have insufficient balancing properties. Thus, the additional current i_b, injected by the balancing circuit (R_b L_b C_b), is necessary to perform an effective balancing process. Due to the resonant character of balancing circuit, the balancing current i_b is triggered only by the f_{SW} harmonic of voltage in node M (u_M). The M-node voltage under the steady state has the following form in the SEPIC converter:

$$u_M = U_{Cout} + U_{CS} - (U_{Cout} - U_{C1})S1(t) - (U_{C1} - U_{C2})S2(t) - (U_{CS} + U_{C2})S3(t). \tag{19}$$

On the basis of (19) it follows that under the balanced state:

$$u_M = U_{Cout} + U_{CS} - U_{SPD}\left(S1(t) + S2(t) + S3(t)\right). \tag{20}$$

In order to analyze behavior of component $S1(t) + S2(t) + S3(t)$, functions Sn can be approximated by the first harmonic of switching frequency (frequency of Sn is f_{SW}). As a result the sum of three $2\pi/3$ phase shifted sinus functions with equal amplitudes is achieved:

$$S1_{(f_{SW})}(t) + S2_{(f_{SW})}(t) + S3_{(f_{SW})}(t) = 0. \tag{21}$$

From (20) and (21) it follows that under the balanced state $u_{M(fsw)} = 0$, therefore the balancing current will not be triggered. Obviously other harmonics exist in u_M but they are not important for the balancing process. Equation (19) can be approximated with the usage of the first (f_{SW}) harmonics of functions Sn:

$$u_{M(f_{SW})} = C\left[(U_{C1} - U_{\text{Cout}})\sin(\omega_{sw}t) + (U_{C2} - U_{C1})\sin\left(\omega_{sw}t - \frac{2\pi}{3}\right) + \right.$$
$$\left. + (-U_{CS} - U_{C2})\sin\left(\omega_{sw}t + \frac{2\pi}{3}\right)\right]. \tag{22}$$

The balanced and unbalanced state varies from each other by the factor determined by ΔU_{C1} and ΔU_{C2} . The formula (22) can be written as:

$$u_{M(f_{SW})} = CU_{SPD}\left[\sin(\omega_{sw}t) + \sin\left(\omega_{sw}t - \frac{2\pi}{3}\right) + \sin\left(\omega_{sw}t + \frac{2\pi}{3}\right)\right] +$$
$$+ C\left[\Delta U_{C1}\sin(\omega_{sw}t) + (\Delta U_{C2} - \Delta U_{C1})\sin\left(\omega_{sw}t - \frac{2\pi}{3}\right) - \Delta U_{C2}\sin\left(\omega_{sw}t + \frac{2\pi}{3}\right)\right], \tag{23}$$

where:

$$\Delta U_{C1} = U_{C1} - U_{C1bal},$$

$$\Delta U_{C2} = U_{C2} - U_{C2bal},$$

U_{C1bal}, U_{C2bal} are voltages for balanced state,

thus:

$$u_{M(f_{sw})} = \sqrt{3}C\left[\Delta U_{C1}\sin\left(\omega_{sw}t + \frac{\pi}{6}\right) + \Delta U_{C2}\sin\left(\omega_{sw}t - \frac{\pi}{2}\right)\right]. \tag{24}$$

For the f_{SW} frequency the balancing current has the same phase shift as the voltage component because the balancing circuit (R_b L_b C_b) is in the resonance with this frequency. Thus, the first harmonic (f_{SW}) of balancing current i_b is given by:

$$i_{b(f_{SW})} = \frac{u_{M(fsw)}}{R_b}. \tag{25}$$

The cycle average current of capacitors C_1 and C_2 caused by the balancing current i_b (i_{in} and i_{Ls} are omitted) with the first harmonic approximation can be derived by combining formulas (17), (18) and (25):

$$I_{Cnib(f_{sw})} = \frac{1}{T_{sw}}\int_t^{t+T_{sw}} -i_{b(fsw)}S_{n(fsw)}dt\,, \tag{26}$$

$$I_{C1ib(f_{sw})} = -\frac{3C^2}{4R_b}\left(2\Delta U_{C1} - \Delta U_{C2}\right), \tag{27}$$

$$I_{C2ib(f_{sw})} = -\frac{3C^2}{4R_b}\left(2\Delta U_{C2} - \Delta U_{C1}\right). \tag{28}$$

The natural current of converter (i_{in}-i_{Ls}) is phase shifted with respect to i_b by -π/2 due to the inductive character of this current. The natural current of the converter (i_{in}-i_{Ls}) causes the cycle average currents of capacitors:

$$I_{CniL\text{in},i_{Ls}(f_{SW})} = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} (i_{\text{in}\,fsw} - i_{Ls\,fsw}) S_{n(fsw)} \mathrm{d}t, \tag{29}$$

$$I_{C1i_{in},i_{Ls}(f_{SW})} = \frac{3\sqrt{3}C^2}{4\omega_{sw}(L_{\text{in}} + L_s)} \Delta U_{C2}, \tag{30}$$

$$I_{C2i_{in},i_{Ls}(f_{SW})} = -\frac{3\sqrt{3}C^2}{4\omega_{sw}(L_{\text{in}} + L_s)} \Delta U_{C1}. \tag{31}$$

Formulas (26) and (31) are true only under the steady state of operating or for changes of state which are slow in relation to transients of i_{in}, i_b, i_{Ls}. In spite of the fact, an *AC* component of natural converter currents i_{in},, i_{Ls} and injected balancing current i_b have rather different magnitudes, their balancing effectiveness can be compared. Balancing by the natural currents of the converter is not effective because it works indirectly. It could be explained on the basis of Equations (30) and (31). The positive ΔU_{C1} could be assumed, which leads to discharging of capacitor C_2. Thus, negative ΔU_{C2} appears and the negative average current starts to flow through capacitor C_1. The fundamental condition for balancing voltages requires the sign of the average current of capacitor C_n to be opposite with respect to the sign of ΔU_{Cn}. It denotes that an undercharged capacitor will be charged and vice versa. This condition is satisfied by the natural converter currents, but their indirect character leads to oscillations (Fig. 7a) of the voltage of flying capacitors which are not acceptable in the real implementation. The oscillations are damped due to the dissipative character of components, but the time constant of this damping may be very long. The balancing current i_b has different influence on the average current of the capacitors. When positive ΔU_{C1} occurs, i_b causes the negative average current of C_1 and twice time lower positive average current of C_2 (as a side effect).

Any deviation of voltage U_{C2} from balanced value will be reduced in a similar manner. It means that the balancing current i_b satisfies the fundamental condition expressed above and moreover it acts almost directly which leads to an effective balancing process without any dangerous oscillations (Fig. 7b). Differences between the balancing process achieved by the natural currents of the converter and the injected current i_b can be noticed also in a steady state operation of the converter. The Fig. 8 presents normalized voltage across flying capacitors versus parallel leakage resistance connected to C_1 for two different series resistance of the balancing branch. The voltages are calculated for the steady state operation of the converter. As previously stated, natural currents of the converter act indirectly and this conclusion can be also proved by comparing Fig. 8a with Fig. 8b.

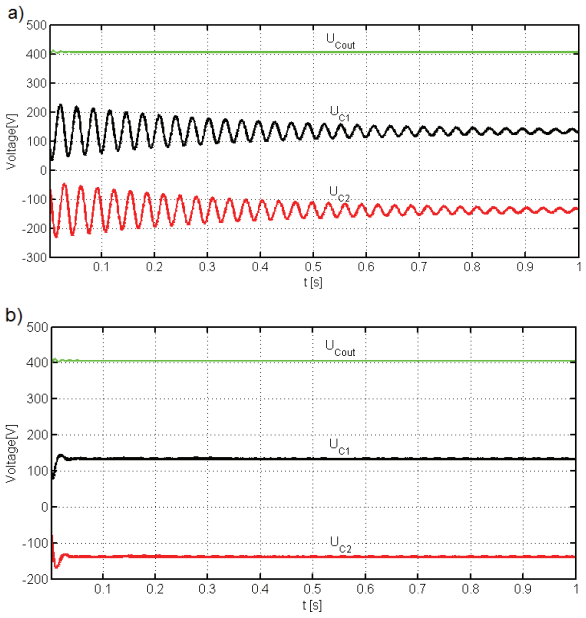

Fig. 7. The voltage across flying-capacitors and output voltage during a balancing process: a) caused only by the natural converter current, b) with the injected balancing current i_b; D = 0.5, P_{out} = 2 kW (R_d = 78.8 Ω). CCM operation. Matlab/Simulink simulation results

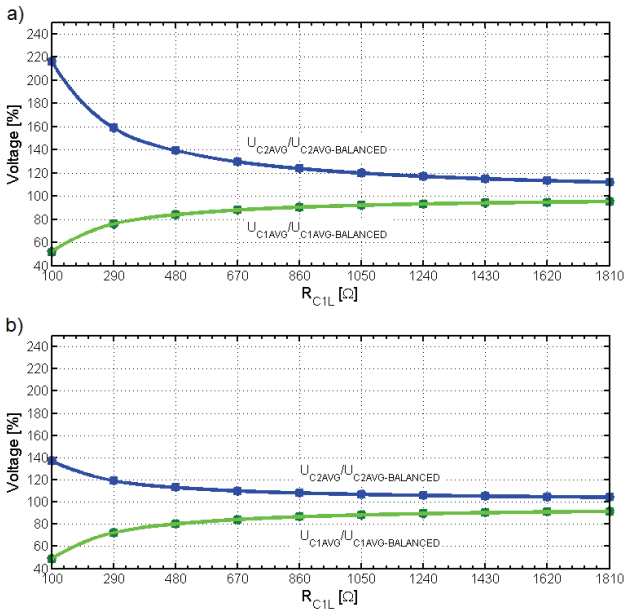

Fig. 8. Balancing effectiveness for two different balancer resistance: a) R_b = 300 Ω, b) R_b = 50 Ω. R_{C1L} is leakage resistance parallel connected to capacitor C_1. U_{out} = 400 V, D = 0.5, P_{out} = 2 kW (R_d = 78.8 Ω). Matlab/Simulink simulation results

Fig. 8a ($R_b = 300\ \Omega$) definitely shows stronger influence of leakage resistance of capacitor C_1 on voltage across C_2. Although the capacitor C_1 has simulated leakage current, the voltage U_{C1} is very close to the proper value. For this high value of R_b the majority of leakage current of capacitor C_1 is provided by the relatively high value of ΔU_{C2}. For lower resistance of balancing branch, natural currents of converter have lower influence on the balancing process. The balancing is more selective in this case. Thus, in the Fig. 8b ($R_b = 50\ \Omega$) voltage U_{C2} is definitely closer to the ideal value and U_{C1} is somewhat further, but generally speaking balancing is more accurate.

All simulation results in this paper have been gained with the use of the Matlab/Simulink software with the SimScape toolbox. Parameters of the model are presented in Table 1 unless otherwise stated in comments to the results. A simulation model utilized the ideal power switches and diodes. No paristic elements were modeled with the exception of inductors, where a series resistance was implemented. Such simplifications lead to results which may be non-accurate when compared to a real converter but they are useful for proving correctness of the presented theoretical analysis and to manifest specific phenomena.

Table 1. Parameters of the simulation model

Parameter		**Value**	
SEPIC inductor 1	L_{in}	1.125	mH
SEPIC inductor 1 DCR	R_{Lin}	100	mΩ
SEPIC inductor 2	L_s	1.125	mH
SEPIC inductor 2 DCR	R_{Ls}	100	mΩ
SEPIC coupling capacitor	C_S	220	uF
SEPIC flying-capacitor 1	C_1	22	uF
SEPIC flying-capacitor 2	C_2	22	uF
SEPIC output capacitor	C_{out}	2200	uF
Balancing inductor	L_b	500	μH
Balancing capacitor	C_b	45	nF
Balancing resistor	R_b	300	Ω
Switching frequency	f_S	33	kHz

4. Conclusions

This paper addressed a problem of balancing of voltages on capacitors of the flying-capacitor DC-DC SEPIC converter. The detailed analysis as well as the simulation results prove that the SEPIC converter has the ability for stable operation as the flying-capacitor converter. Furthermore an application of the balancing circuit makes it possible to achieve natural voltage balancing of the flying capacitor voltages. The paper presents an original analysis that shows the difference in the balancing phenomena by a natural internal current of

a converter and the current of the balancing booster. A specific indirect action of the internal current of the converter on the capacitor voltages under the unbalanced state is described. Also a favorable impact of the balancing booster on the reduction on oscillations in the converter was discovered.

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