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Analysis of High-Performance Near-threshold Dual Mode Logic Design

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***Abstract*—A novel dual mode logic (DML) model has a superior energy-performance compare to CMOS logic. The DML model has unique feature that allows switching between both modes of operation as per the real-time system requirements. The DML functions in two dissimilar modes (static and dynamic) of operation with its specific features, to selectively obtain either low-energy or high-performance. The sub-threshold region DML achieves minimum-energy. However, sub-threshold region consequence in performance is enormous. In this paper, the working of DML model in the moderate inversion region has been explored. The near-threshold region holds much of the energy saving of sub-threshold designs, along with improved performance. Furthermore, robustness to supply voltage and sensitivity to the process temperature variations are presented. Monte carol analysis shows that the projected near-threshold region has minimum energy along with the moderate performance.**

***Keyword*—CMOS logic, dual mode logic, dynamic mode, high performance, minimum energy point, near-threshold**

I. INTRODUCTION

OVER the last four decades, enrichments in research are being used to obtain a design optimization in the logic circuit to achieve minimum-energy point (MEP). However, circuit performance becomes an issue, it needs to come out of minimum-energy point in order to achieve a significant improvement in high performance [1]. Nowadays, researchers are targeting a unique design under the lower technologies to optimize energy and the speed, a pareto-optimal design curve for optimized operating point (OOP) is as shown in Fig. 1. It exclusively describes the minimum delay required for a given energy (and vice versa) over a set of design parameters such as the threshold, supply voltage and size of a transistors [2]–[6].

Since last 30 years, the device parameters have been scaled down to achieve lower power consumption. However, scaled technologies reduces the device parameters like supply voltage, threshold voltage and gate oxide thickness. As a result, the scaled technology suffers from severe problems. Firstly, performance is reduced due to threshold variations at low power supplies. Secondly, a low-V_{th} device increases the sub-threshold leakage current exponential. It increases by ten times for every 0.1-volt reduction of V_{TH} [7], [8]. As device parameters scale down, leakage current in a sub-micron region turn out to be significant and comparable with dynamic power dissipation. Further, scaling of supply voltage leads to performance degradation, less robustness to temperature variations and process deviation [9]–[11]. High performance can be accomplished only at higher supply voltages. However higher supply voltages leads to increased power consumption [12]. These problems can be solved through a novel mixed-mode design [13], multi-threshold voltages [14] and dual supply voltages [15].

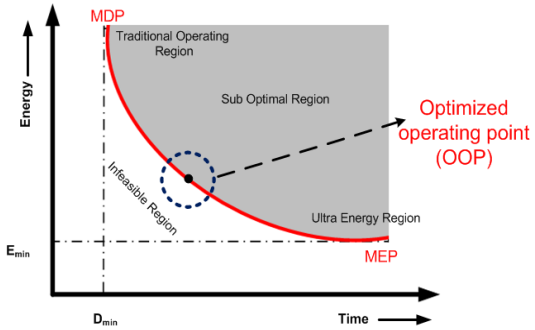

Fig 1. Optimized operating region of a pareto-optimal design curve

The DML models that have been proposed recently can switch between dynamic and static modes through an asymmetrical clock based on the real-time system requirement. As a result, DML model achieves enhanced trade-off between power dissipation and performance. In dynamic mode of operation, DML model attains very high speed though increased power consumption. In static mode, low supply voltage DML model achieves lower power dissipation along with modest performance [16], [17].

In this paper, we explore the dual mode design in near-threshold operation to accomplish optimized power dissipation and propagation delay. Various benchmark circuits have been taken, such as standard logic gates, multiplexer, chain of inverters and full adder carry cell. These circuits are realized with cadence virtuoso simulator, at super-threshold and near-threshold regions. Furthermore, Monte carol analysis has been executed to find out the standard deviation σ (sigma) for threshold voltage variations.

This paper has been divided into five sections. The brief introduction part of the paper is followed by an elaborate discussion of near-threshold design in section 2. The DML design and principle of operation are presented in Section III. In Section IV, near-threshold DML circuit simulation set-up, results are discussed. Finally, the conclusions are presented in Section V.

II. NEAR-THRESHOLD MODEL4

Energy efficiency can be obtained when CMOS designs operate at near the threshold voltage. Based on the transistor ON-current, a propagation delay model has been obtained. This model has been applied in DML designs to determine the minimum-energy point [18], [19].

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In modern CMOS logic, energy consumption mainly depends on charge and discharge of inner node capacitances, which can be minimized by scaling of supply voltage. However, the lower limit of the supply voltage in commercial applications is usually around 70% of the nominal supply voltage. This lower limit is dictated by concerns about performance and robustness loss [20], [21]. In a wide range of voltage scaling techniques, determining an optimal region in the energy per operation is crucial for achieving desired optimized energy and delay. In Fig. 2, the energy-delay optimized curve has been shown. The super-threshold region ($V_{DD} > V_{TH}$), energy depends highly on the supply voltage and it rises exponentially due to switching energy. Therefore, voltage scaled down to the near-threshold region ($V_{DD} \sim V_{TH}$) produces energy saving in the order of 10X at the cost of around 10X performance loss. However, scaling down further to the sub-threshold region ($V_{DD} < V_{TH}$) leads to an exponential increase in propagation delay, source more leakage current. The increased leakage current dominates any reduction in switching energy and turn out to be more significant [22]–[24]. A simple experimental trans-regional expression for ON-current and delay in the NTC region is as follows. In the saturation region with $V_{DT} > 0$, I_{on} is estimated with the α-power law model [25].

$$I_{on} = k_1 w V_{DT}^{\propto} \tag{1}$$

where I_{on} is the current at $Vgs = Vds = V_{DD}$. ON-current depends on ($V_{DD} - |V_t|$), which can be denoted by V_{DT}, k_1 is process parameter, W is width of a transistor, α is velocity saturation index (approximately 1.3 – 1.5 nm). In the sub-threshold region with $V_{DT} < 0$, I_{on} is estimated with an exponential model [26].

$$I_{on} = I_0 w e^{\frac{V_{DT}}{nV_T}} \tag{2}$$

where I_0 is the current per unit width at $V_{DT} = 0$, V_T is the thermal voltage (kT/q, 29.6 mV at 70 ºC), and n is the sub-threshold slope factor. Markovic proposes for a near-threshold current expression derived from EKV [18] is

$$I_{on} = \frac{2nC_{ox}}{k_{fit}} \frac{W}{L} V_T^2 \left[ln\left(e^{\frac{(1+\eta)(V_{DD}+V_t)}{2nV_T}} + 1 \right) \right]^2 \tag{3}$$

However, this model has been problematic and is also complicated to understand. In trans-regional on-current model, the curve is almost straight for $V_{DD} < V_t$, conforming to the exponential I-V relationship [23]. Above V_t, the curve moves off. The ON-current is closely fitted using the following equation:

$$I_{on} = I_0 w e^{\frac{V_{DT} - aV_{DT}^2}{nV_T}} \tag{4}$$

The expression is conveyed a quadratic dependency on V_{DT} rather than supply voltage. So, a change in V_t due to body bias or process deviation do not impact fitting parameters for a new value (for a, n, or I_0). Generally, the propagation delay of a gate can be estimated as

$$t_{pd} = k_2 \frac{C_{Load} V_{DD}}{I_{on}} \tag{5}$$

Trans-regional delay model, from equation (4) and (5) a modest expression for gate-delay dependency on V_{DD} at the near-threshold region is

$$t_{pd} = k \frac{C_{Load} V_{DD}}{w} e^{\frac{-V_{DT} - aV_{DT}^2}{nV_T}} \tag{6}$$

The propagation delay is more delicate to small current when transistors are partially ON as input rises [27]. The minimum-energy operational region by the trans-regional model, the analysis is homogeneous to the Calhoun [28] and Zhai [29] which is a superior model for OFF-current. The total energy is

$$E_{Tot} = E_{dyn} + E_{leak} \tag{7}$$

The dynamic energy is

$$E_{dyn} = C_{dyn} V_{DD}^2 \tag{8}$$

where C_{dyn} is actual switching capacitance of the complete circuit. The leakage energy is

$$E_{leak} = I_{off} V_{DD} T_C \tag{9}$$

I_{off} is the leakage current when $Vgs = 0$ and $Vds = V_{DD}$. Calhoun [28] approximated I_{off} as I_{on} at $V_{DD} = 0$.

$$I_{off} = I_1 W_{eff} e^{\frac{\eta V_{DT}}{nV_T}} \tag{10}$$

Finally, the total energy of the circuit is

$$E_{Tot} = C_{dyn} V_{DD}^2 \left[1 + R e^{\frac{\eta V_{DT}(1-\eta) - aV_{DT}^2}{nV_T}} \right] \tag{11}$$

With $R = C_{leak}/C_{dyn}$ it can be shown that the minimum energy point can be obtained by differentiating energy with respect to V_{DD}. The sub-threshold region, leakage and delay have more sensitivity to the threshold (V_t), so the minimum-energy region is autonomous of V_t. Nevertheless, in near-threshold operation, equation (11) shows that increasing V_t reduces the leakage more than it rises. Therefore, the minimum-energy region ensues at the lower supply voltage.

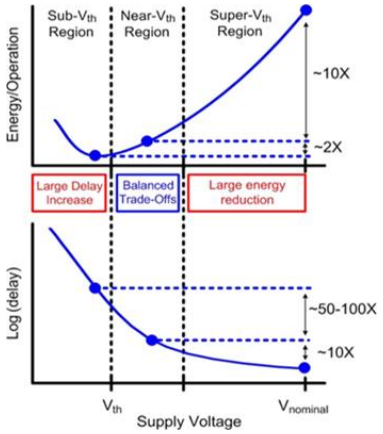


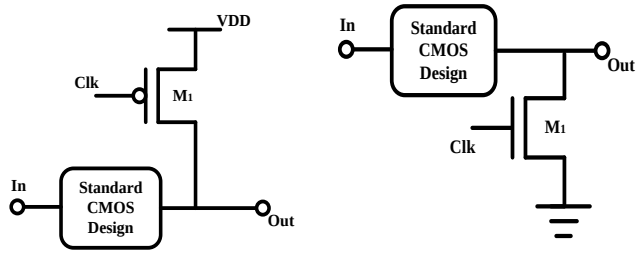
Fig 2. Energy delay optimized curve [22]

III. PRINCIPLE OPERATION OF DML DESIGN

The DML design has a novel configuration that uniquely incorporates the advantages of the static and dynamic mode approaches. Static mode DML functions similar to static CMOS accomplishing ultra-low power dissipation along with adequate performance. Dynamic mode DML is connected with an external asymmetrical clock, which gives very high performance along with the increased power dissipation. The distinctive feature of the DML circuit offers the choice to control real-time system performance trade-off between speed and energy [30].

The basic design of DML is alike to a conventional CMOS logic with an additional transistor M1, whose gate terminal has been joined with an external asymmetrical clock pulse, is as shown in Fig. 3. At first sight, DML structure seems equivalent to a noise tolerant precharge (NTP) configuration. However, the advantage of high performance and high-noise-tolerance in dynamic logic distinguishes DML from NTP. The main aim of

the DML gate is to operate in two efficient functional modes by gaining the advantage of both power dissipation and performance. The DML design is divided into two types, namely DMLA model and DMLB model. DMLA model has an extra PMOS transistor associated in parallel to pull-up network, in between power supply and output node, which precharge the output node to high voltage (logic one). DMLB model has an extra NMOS transistor connected in parallel to pull-down network, during the precharge period, which precharge output node to a logic low [16].



(a) (b)

Fig 3. DML basic block diagram a) DMLA model and b) DMLB model

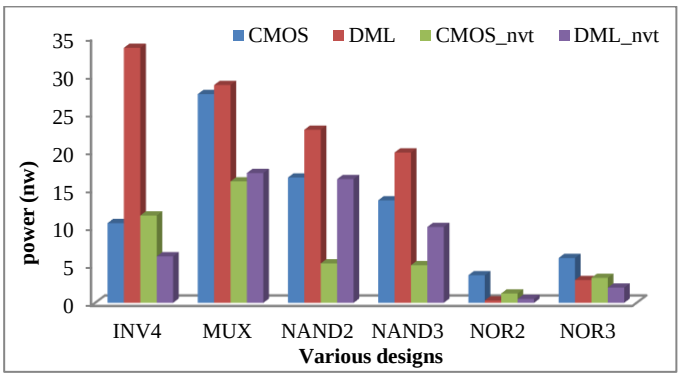
DML gate operates in dynamic mode when the asymmetric clock signal is given to gate terminal of the extra M1 transistor, providing two dissimilar modes: precharge and evaluation mode. In precharge mode, a circuit output node is precharge to logic high in DMLA model and to a logic low in DMLB model. During the evaluation mode, the circuit output node is measured corresponding to inputs of the circuit. DML circuit works as conventional CMOS in static mode while keeping the asymmetrical clock constantly higher in the case of DMLA model and continually lower for DMLB model. As a result, it operates similar to CMOS while excluding the outward parasitic capacitance, which is generally unimportant. DML circuit functioning in dynamic mode has numerous benefits as compared to the basic dynamic logics [17], [31]. DML circuit eradicates the domino logic complications such as charge sharing, high power consumption, and exposition to glitches. These problems increase even more with scaling down of the device parameter. Since an additional precharge transistor is kept in corresponding to stacked transistor, the evaluation process made over these transistors; this decreases the transaction delay between the high to low logic levels. To reduce the intrinsic capacitances, the stacked transistors are sized with minimal width. As a result, dynamic mode function increases the performance while the static operation has moderate performance. The sized transistor also decreases the power dissipation when equated with basic CMOS design. The additional precharge transistor is scaled to the minimum size in order to reduce leakage currents [32].

IV. PROPOSED NEAR-THRESHOLD DML CIRCUITS

The DML circuits have been proposed in order to exploit the advantages of the static and dynamic mode operations. However, the DML design incurs certain propagation delay in static mode and moderate power dissipation in dynamic mode. Unfortunately, the DML design operating in sub-threshold region has increased propagation delay and leakage power. Hence, the sub-threshold design has been degraded to niche markets due to its key performance consequences. Therefore, the DML designs are analyzed in the near-threshold region in order to optimize the energy and performance.

A. Benchmark Circuits

Functioning of DML circuits in near-threshold region has been discussed. Various logic benchmark circuits have been verified such as basic NAND and NOR gates with 2 and 3 inputs, 2 to1 multiplexers, and sequence of four inverters. A sequence of four inverters is designated as an inverter is commonly used in digital circuits. The inverter transistors size is chosen to have equal fall and rise times in each stage. To implement these designs, cadence virtuoso simulator has been used with gpdk 45 nm. The near threshold design function has the supply voltage at 600 mV, which is close to the threshold voltage of a transistor. Basic CMOS and DML designs were compared in terms of the power dissipation and the propagation delay times, which are shown in Fig. 4. In all the designs, DML dynamic model has lower propagation delay and the near-threshold design increases the delay time as compared to conventional design. However, near-threshold DML has reduced power as equated to conventional design.



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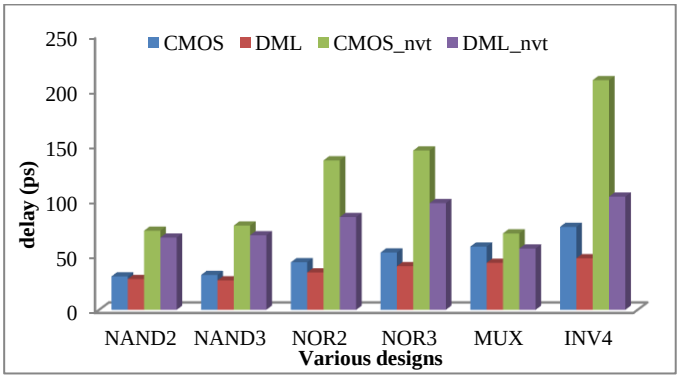
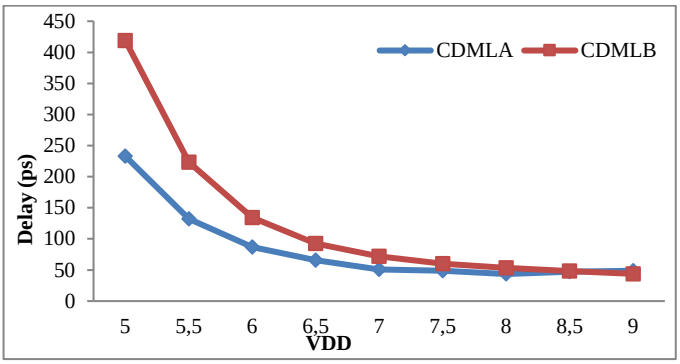


(b)

Fig. 4. Near-threshold designs (a) Power dissipation and (b) Propagation delay.

A full adder is one of the examples of a classic complex CMOS gate. As carry cell drives the sum output in a full adder, DMLA and DMLB carry cells have been analysed in terms of leakage current, propagation delay, and power dissipation which are shown in Fig. 5. DMLA design has low leakage and reduced delay times with moderate power consumption as compared to DMLB carry cell design.



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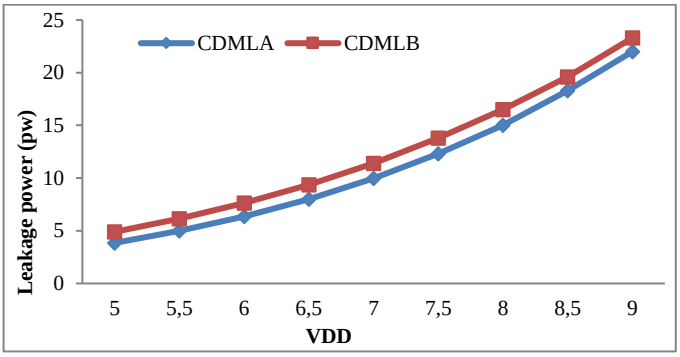

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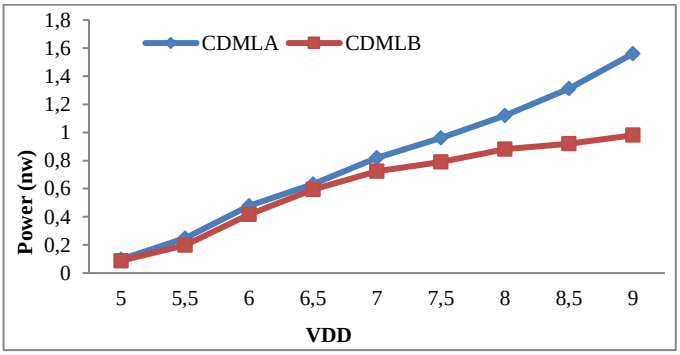


(c)

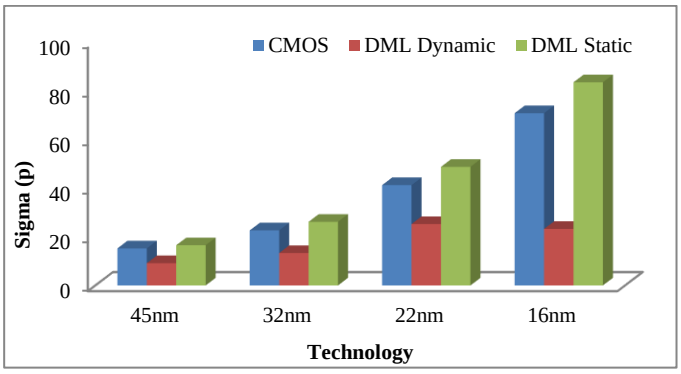
Fig. 5. Carry cell, VDD vs (a) Propagation delay (b) Leakage power (c) Power dissipation

B Monte Carlo Analysis

Monte carol analysis has been performed in order to find the sigma at the threshold voltage variation of 10 %. The supply voltage 500 mV is considered for the near-threshold operation, which is around the threshold voltage of the transistors. Various parameters of the PTM High-Performance files are as given in Table I. Basic NAND gate with three inputs has been considered to calculate the sigma in super-threshold and near-threshold designs. Fig. 6 shows that DML dynamic model attains lower sigma as compared to basic CMOS design whereas DML static exhibits a slight increase in sigma. A lower sigma value has been observed for 16 nm technology at the near-threshold operation. A minimum delay of the near-threshold design for each technology has been measured and is shown in Fig. 6(c). It has been observed that DML dynamic model attains higher performance as compared to CMOS.

TABLE I
VARIOUS PARAMETERS OF THE PTM HIGH PERFORMANCE

	16 nm	**22 nm**	**32 nm**	**45 nm**
V_{tn} (V)	0.47965	0.50308	0.49396	0.46893
V_{tp} (V)	-0.43121	-0.4606	-0.49155	-0.49158
V_{DD} (V)	0.7	0.8	0.9	1.0
t_{ox}_nmos (nm)	0.95	1.05	1.15	1.25
t_{ox}_pmos (nm)	1.0	1.1	1.20	1.30



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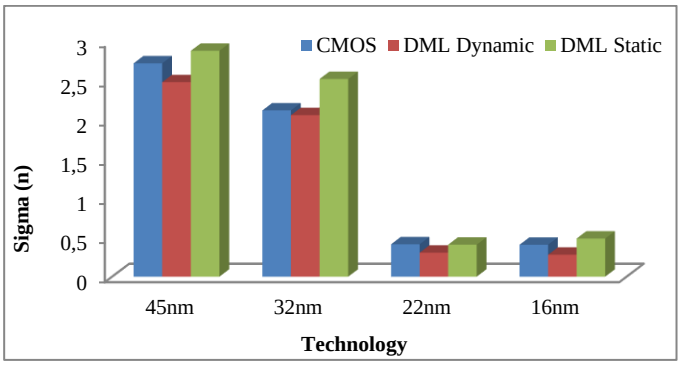

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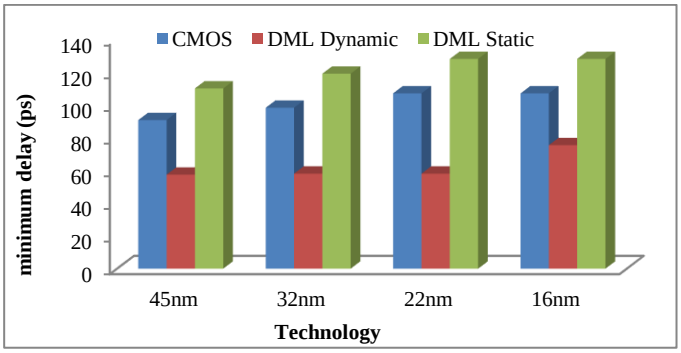


(c)

Fig. 6. Monte Carlo analysis (a) Super-threshold (b) Near threshold (c) Minimum delay

C. Multi-Threshold Design

Multi-threshold design contains high-V_{th} and low-V_{th} transistors. The high-V_{th} transistor reduces the leakage current in an ideal state. Low-V_{th} transistors switch faster and hence it

increases the performance [33]. The main advantage of the multi-threshold design is having the high-V_{th} and low-V_{th} in the same chip [34]. In DML design additional transistor play very important role in high to low output transition in DMLB model and low to high transition in DMLA model. We have proposed and examined the additional transistor by applying the multi-threshold voltages. Low-V_{th} transistor achieves very low propagation delay due to fast transition between high-to-low logic of output node. Furthermore, other threshold voltage combinations of DMLB model have been observed and which are given in Table 2. Simulation results shows that the dynamic mode operation attains low PDP up to 36-57% as compared to static DML model and list numbers are highlighted with a bold letter.

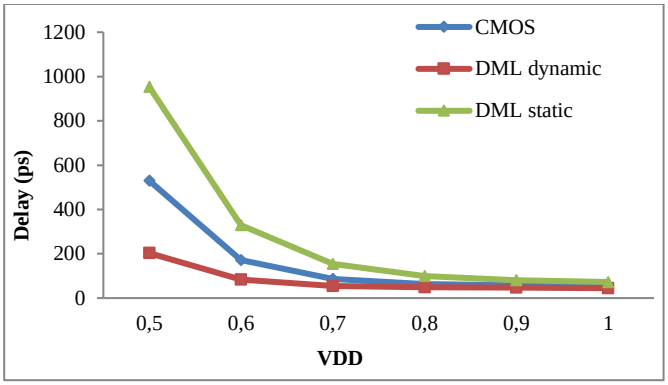
TABLE II
VARIOUS THRESHOLD VOLTAGE COMBINATIONS

Combinations	*Power(nW)*	*Delay (pS)*	*PDP(aJ)*
N3, V_{tL} Dynamic	199.6	34.9	6.98
N3, V_{tL} Static	193.8	83.6	16.2
N3, V_{tH} Dynamic	142.9	52.3	7.47
N3, V_{tH} Static	138.1	83.9	11.6
All N,V_{tL} Dynamic	232.3	33.4	7.75
All N, V_{tL} Static	222	61.3	13.6
All N, V_{tH} Dynamic	139.5	57.3	7.98
All N, V_{tH} Static	134.2	122.1	16.4
All P, V_{tL} Dynamic	286.4	3.29	9.41
All P, V_{tL} Static	262.4	76.4	19.5
All P, V_{tH} Dynamic	141.4	57.5	8.12
All P, V_{tH} Static	136.5	100	13.7

Note: V_{tL}- low threshold voltage, V_{tH} -high threshold voltage

D. Supply voltage variations

The supply voltage plays a major role in high performance designs, in order to analyze variation in propagation delay times with respect to region of operation. The supply voltage is varied from 0.5 to 1 V. The basic NAND and NOR gates have been implemented with three and four inputs. Detailed graphs for supply voltage versus propagation delay are as shown in Fig. 7. The propagation delay rises exponentially as the supply voltage is reduced beyond 600 mV. The DML dynamic design achieves lower propagation delay whereas DML static design shows a slight increase in propagation delay as compared to basic CMOS design. To control further delay, the design should not be operated in lower supply voltages. However the design can be considered with supply voltage up to the near-threshold for the optimized speed and power.



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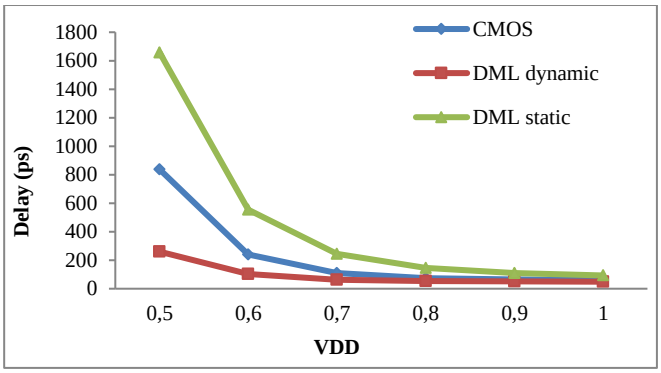

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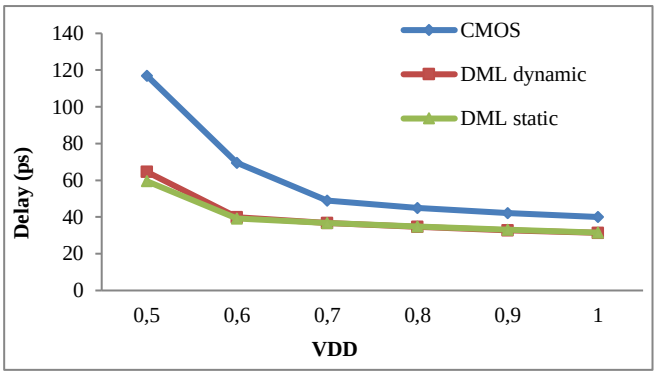

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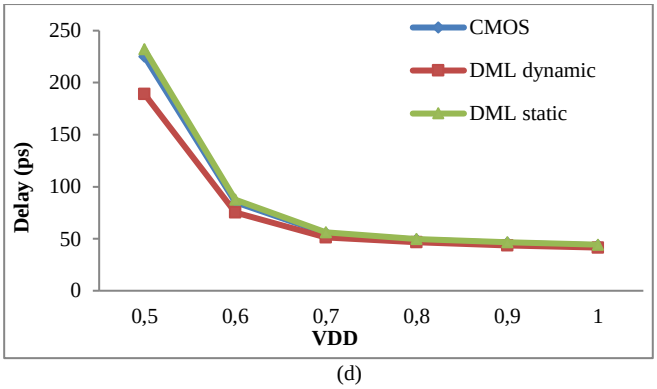
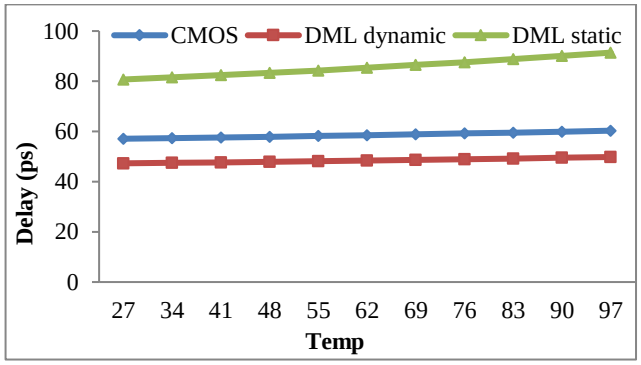


(d)

Fig 7. Propagation delay versus VDD (a) NAND3 (b) NAND4 (c) NOR3 (d) NOR4

E. Thermal variations

Another important parameter in nanotechnology is the thermal variations. Fig. 8 shows the temperature variations of basic NAND and NOR gates with 3 and 4-inputs. As temperature is varied from 97 °C down to 27 °C, it was noticed that there is a slight increase in the delay as temperature increases. Further, DML dynamic model exhibits lower delay among the all designs. However, DML static model has marginal increase in delay as compared the basic CMOS.



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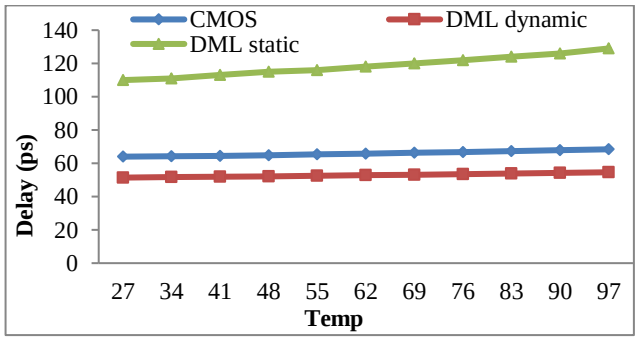

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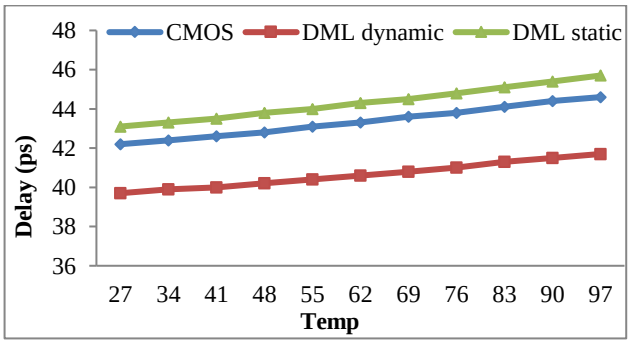

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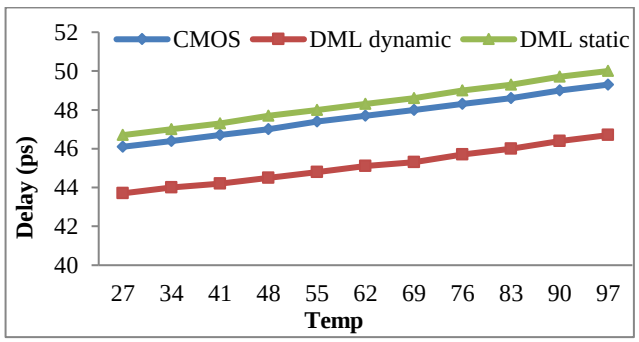

(d)

Fig 8. Propagation delay versus temperature (a) NAND3 (b) NAND4 (c) NOR3 (d) NOR4

V. CONCLUSION

In this paper, we have explored the near-threshold operation in order to optimize the energy and performance trade-off. Recently proposed DML model has been designed to operate in optimized operating point to recover some of the lost performance while preserving the minimum-energy point. The existing model use lower technologies that suffer from robustness to supply voltage and sensitivity to the process temperature variations. To analyze these effects, we choose 45 nm gpdk and 16 nm PTM high-performance files. The benchmark circuits such as basic universal gates, multiplexer, and chain of inverters have been implemented. In the proposed design, a supply voltage of 500 mV is taken as the supply voltage for operating in near-threshold design. Various PTM HP files have been considered in order to study the effect of scaling and the results are presented in graphs. Simulation result shows that the projected near-threshold DML design attains minimum power along with the improved performance as compared with CMOS circuits. However, delay increases in sub-threshold region and power increases in the super threshold region. Therefore, a design with supply voltage close to the near-threshold value can achieve optimized power and performance.

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